MEDELEC

FOR-4.2

RECORDING OSCILLOSCOPE

SM38.77.1

MP MASTER
MA23324

FOR-4.2

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SM38.77.1

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RECORDING OSCILLOSCOPE FOR-4.2 HANDBOOK CONTENTS

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LIST OF CIRCUIT DIAGRAMS

C6/13774	Block Diagram FOR-4.2
C/12448/1	Sweep Velocity Circuit
C/12446/1	Display Board Circuit
C2/13505/1	Display Focus and Brilliance Circuit
C2/13500/1	Camera Focus and Brilliance Circuit
C/11668/1	Camera Cassette Circuit
C/12447/1	Camera Control Board Circuit
C6-083-14819	Main Circuit DFO6M Mk. II
CD-072-14771-1	Indicator Board
C/11707/1	Power Unit Circuit
C/11460/1	Stabiliser Circuit
C/11456/1	Stabilised EHT Supply Circuit
C/11458/1	Audio Amplifier Mk. III Circuit
CD-043-14242/1	FOR-4.2 Y Amplifier Circuit
CD-043-14243/1	FOR-4.2 X Amplifier Circuit
CD-043-14245/1	FOR-4.2 Trigger Circuit
A1-043-14851	FOR-4.2 General Circuit

Serial No.....

AMENDMENTS FOR-4.2

Issue 1

RECORDING OSCILLOSCOPE FOR-4.2

1.0 INTRODUCTION

1.1 The FOR-4.2 provides 4-channel display and recording facilities suitable for many instrumentation, control and monitoring applications. Apart from its use as a normal oscilloscope, it may be used in the single frame modes as a storage oscilloscope or X-Y plotter and in the continuous motion modes as a replacement for a UV galvanometer recorder. The recording technique, perfected by Medelec in the medical instrumentation field, employs a fibre-optic tube to give a high definition, direct image on daylight developing or darkroom processed paper. Permanent records are produced at a fraction of the cost of usual photographic techniques.

1.2 The fast response time associated with an inertialess indicator and the range of timebase speeds allow detailed examination of transients (5μs per cm) and trend recording (down to slower than 2s/cm). The Superimposed recording mode easily shows 'spread' on repetitive signals. The Raster mode provides maximum duration using minimum length of paper but retaining good time resolution. The paper drive motor is servo controlled, giving accurate speeds independent of power line frequency and voltage variations.

1.3 The large monitor screen is always visible and provides an exact duplicate of the image being recorded; with the exception of FOCUS and BRILLIANCE, common controls operate on both CRT's. External X deflection and Z modulation facilities permit correlated recording of up to six variables. The horizontal deflection circuit has a wide range of triggering modes and a velocity range from 5μs/div to 0·5 minutes sweep time. A built-in audio amplifier and speaker enables any applied Y signal to be audibly monitored. Four identical vertical deflection amplifiers are provided, carefully matched for gain and phase shift. These are preceded by compensated attenuators which offer an input impedance of 1MΩ at any semsitivity. This simplifies matching of the four x 1, x 10 probes supplied.

2.0 SPECIFICATION

RECORDING CATHODE RAY TUBE

Type:	GEC 1358X single gun with helical PDA. High resolution flat fibre-optic faceplate 10 x 8cm.
Phosphor:	BE (P11), blue, short persistence.
EHT:	6kV (overall)

MONITOR CATHODE RAY TUBE

Type:	GEC 1824A single gun with helical PDA.
Display:	Flat faceplate 14 x 11·4cm.
Phosphor:	GH (P31), green, short-medium persistence (on GEC 1824A). GM (P7), dual layer long persistence (on GEC 1846A) available to order.
EHT:	6kV (overall).
Graticule:	10 x 8 divisions (14mm per division) with continuously variable edge illumination.

VERTICAL AMPLIFIERS

Each vertical (Y) amplifier has the same characteristics, but with independent controls.

Bandwidth:	DC coupled, DC to 125kHz (< -3dB) AC coupled, 1·6Hz to 125kHz (< -3dB).
Sensitivity:	10mV/div to 50V/div in 12 calibrated steps. Variable preset control to reset against calibrator. 1mV/div using x 10 facility.
Accuracy:	±5%
Input Impedance:	1MΩ + 30pF (via BNC socket)

Input Coupling:	DC, AC, ground reference.
Maximum Input:	±400V AC peak or DC.
Y Shift:	13 divisions.
Channel Selection:	Y1 only; Y1 and Y2; Y1, Y2, Y3 and Y4. Beam switch runs at 100kHz to 400kHz.
Audio Monitor:	Signals from one or more vertical deflection amplifiers may be selected by push-button for audio monitoring. A volume control is provided and the output will drive an internal or external loudspeaker of from 3Ω to 15Ω impedance. Power output is approximately 2 Watts.

TIMEBASE

Free-running or triggered.

Ranges:	50μs/div to 0·5s/div in 14 calibrated steps. Variable control (with indication of uncalibrated operation) and x 10 expansion on X axis extends ranges from 5μs/div to 2·5s/div.
Accuracy:	±5% (basic ranges)

TRIGGER

Trigger Selection:	Internal, from Y1, Y2, Y3 or Y4 or any combination. External, via BNC socket. Coupling, AC or DC, positive or negative.
Trigger Sensitivity:	100mV (external), < 0·2 div (internal).
Trigger Level:	Continuously variable to 60V.
Trigger Output Impedance:	500k//30pF
Trigger Operation:	Normal, from trigger level control; auto, trigger level scaled to input signal level.

HORIZONTAL AMPLIFIER

Bandwidth:	DC to 125kHz (< −3dB) without expansion. Phase shift relative to Y amplifiers < $2·5^{o}$ at 50kHz.
Sensitivity:	10mV/div to 20V/div in 9 steps. Variable preset control to reset against calibrator.
X Expansion:	Switched x 10 expansion, symmetrical about the centre of the screen.
Accuracy:	±5%
Input Impedance:	1MΩ + 30pF (via BNC socket)
Maximum Input:	±400V AC peak or DC
X Shift:	Allows any part of a fully expanded trace to be centred.

BRILLIANCE MODULATION (Z)

Input:	±12V maximum. Positive input brightens trace. At the correct brilliance setting, 1V to 2V (pk-pk) gives optimum grey scale.
Input Impedance:	100kΩ (via BNC socket).

RECORDING FACILITIES

Modes:	Single Sweep, Superimposed Sweeps, Raster, Continuous, with RECORD switch or FOOTSWITCH control.
Paper:	100mm width Linagraph direct print.

Paper Speeds:	0·5, 1,2, 5, 10, 20, 50, 100cm/s. Divide by 10 and divide by 50 options are available. Intermediate speeds by remote control.

POWER REQUIREMENTS

Voltage:	100 to 125V or 200 to 250V, +10%, −20%
Frequency:	50 to 60Hz
Power:	66VA approximately.

DIMENSIONS

Bench Case (overall)

Height:	340mm (13·4 inches)
Width:	450mm (17·8 inches)
Depth:	600mm (23·6 inches)
Weight:	34kg (75lbs)

3.0 OPERATING INSTRUCTIONS

3.1 Control Functions

The control functions will be described working from left to right across the display panel and then across the amplifier panel.

3.1.1 Display Panel Controls

SPEED (mm/sec)

This column of five push-buttons controls the speed of the paper drive motor. The speeds shown express the rate of movement of the paper past the face of the cathode ray tube. The top buttons select the paper speed; the bottom button switches the multiplier. The multiplier button is a push lock/push release button. The remaining buttons lock when pushed in and are released when an adjacent button is pressed. Two or more buttons may be pressed simultaneously; the paper speed will then be the sum of the indicated speeds but will not give a paper speed faster than 1000mm/s.

MODE

This column of five push-buttons controls the recording mode. The upper four buttons lock when pushed in and are released when an adjacent button is pressed. The bottom button is a push lock/push release type. The recording modes are:-

S.S.	Records are taken during a single sweep of the timebase on stationary paper.
SUP	Records are taken over a number of sweeps of the timebase on stationary paper.
RASTER	Records are taken over a number of sweeps of the timebase on moving paper.
CONT	Vertical deflection signals are transferred to the horizontal deflection plates and records are taken on moving paper over any desired period.
SPACE	The paper will move on by one screen height each time the button is pressed. When the button is locked in, the paper will move on by one screen height whenever the RECORD button or FOOTSWITCH is released and when the mode is changed from RASTER or CONT to any other mode.

POWER

This push on/push off button switches the a.c. power to the instrument and provides mechanical indication of power ON and OFF. An associated lamp indicates power ON.

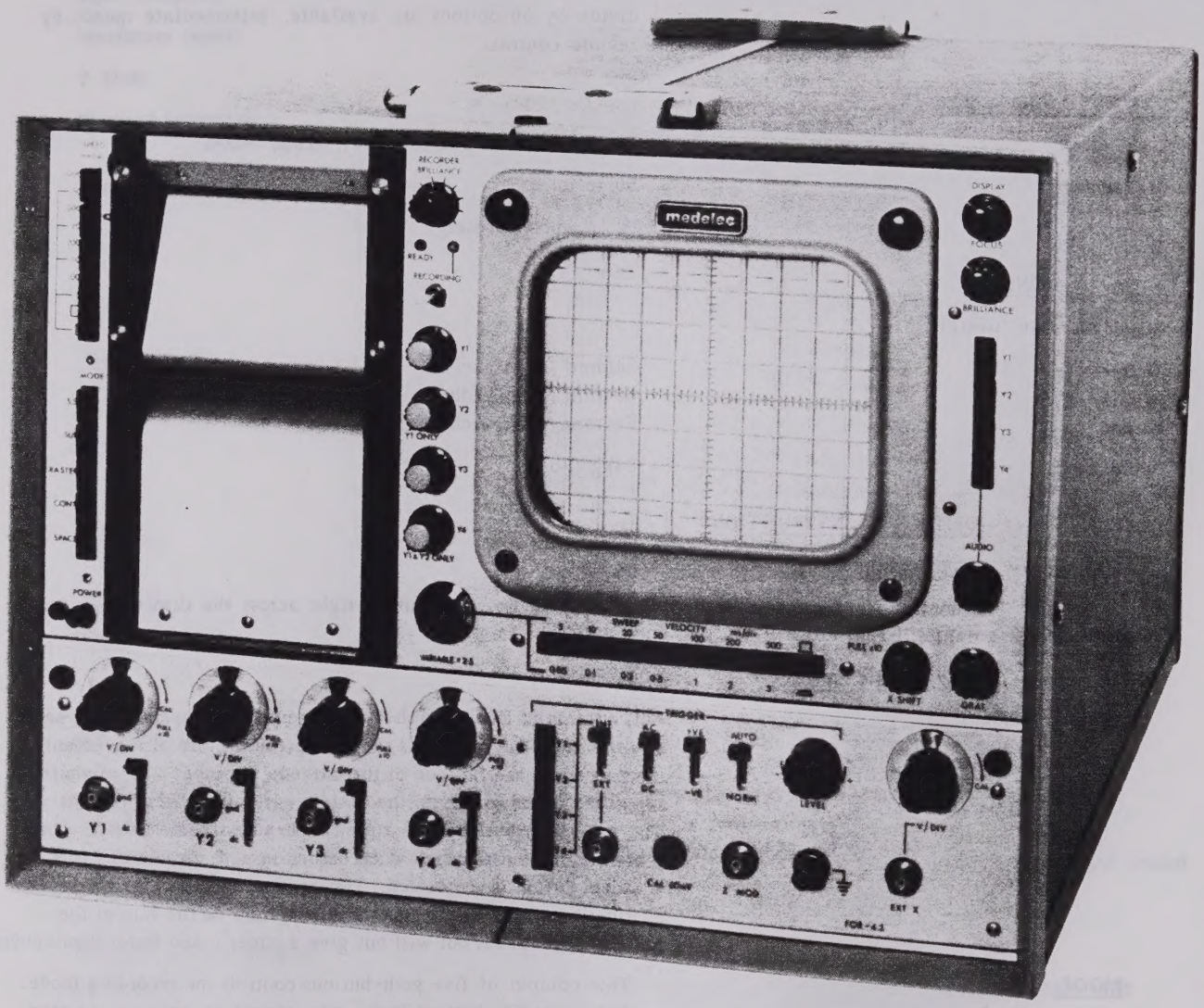


Fig. 3.1 Front Panel Diagram

RECORDER BRILLIANCE

This potentiometer controls the brilliance of the record CRT. Graduations are engraved on the panel to assist in resetting the brilliance for specific recording conditions. NOTE: The focus control for the record CRT is adjusted by an edge wheel controlled potentiometer. The knurled wheel is situated in the right-hand side of the record CRT recess and is accessible when the paper cassette is opened to reveal the face of the CRT.

READY

This LED indicates that the system is primed ready to make a recording.

RECORDING

This LED indicates that the system is in process of making a recording. The associated 3-position toggle switch may be used to provide the record command signal. The switch is biased against the lower position but may be left in the upper position when the recorder requires to be continuously primed, e.g., for Superimposed, Raster or Continuous modes.

Y1, Y2, Y3, Y4

These four potentiometers may be adjusted to provide the required vertical positioning of the four beams. When the Y4 control is turned fully counter-clockwise (Y1 and Y2 ONLY), the Y3 and Y4 traces will be switched off and only Y1 and Y2 will be displayed with increased brilliance. When the Y2 control is turned fully counter-clockwise (Y1 ONLY), only the Y1 trace will be displayed with a further increase in brilliance.

SWEEP VELOCITY (ms/div)

This group of eight push-buttons selects the sweep velocity. The extreme right-hand button (push lock/push release) switches the x 100 multiplier. The remaining buttons lock when pushed in and are released when an adjacent button is pressed. Two or more buttons may be pressed simultaneously; the sweep velocity will then be the sum of the velocities indicated by the depressed buttons.

VARIABLE x 2·5

This potentiometer provides fine adjustment of sweep velocity up to x 2·5 of the indicated velocity. The sweep velocity is calibrated with the control in the fully counter-clockwise switch position.

FOCUS

This potentiometer adjusts the focus of the display CRT.

BRILLIANCE

This potentiometer adjusts the brilliance of the display CRT.

Y1, Y2, Y3, Y4

This group of four push buttons selects the vertical deflection signals for audio monitoring. The buttons lock in when pressed and release when an adjacent button is pressed. If two or more are pressed simultaneously, the sum of the selected signals will be amplified for audio monitoring. There is no interaction on the display tube when audio signals are summed.

AUDIO

This potentiometer controls the volume of the audio signal.

GRAT

This potentiometer controls the intensity of illumination of the graticule.

X SHIFT

This potentiometer provides simultaneous horizontal movement of the four traces. When the control knob is pulled out, it operates a switch to increase the gain of the horizontal amplifier x 10. Expansion is symmetrical about the centre vertical graticule line.

3.1.2 Amplifier Panel Controls

V/DIV

This control performs three functions. The rear knob selects the sensitivity range of the amplifier. The front knob provides smooth control of the amplifier sensitivity over a range of approximately 2·5:1. The amplifier is calibrated with the control in the fully clockwise, switched position. The front knob may also be pulled out to increase the sensitivity of the amplifier x 10. There are four controls of this type on the module, one for each Y channel.

Y1, Y2, Y3, Y4

These BNC sockets provide the input connections for the four vertical deflection amplifiers.

ac - gnd - dc

These four 3-position switches select ac or dc coupling or the input earthed. In the earthed position, the amplifier input is earthed and the input socket is disconnected.

TRIGGER

The group of four buttons defines the source of the internal trigger signal. This may be taken from any one of the four vertical deflection channels, whether that channel is displayed or not. The buttons are of the push lock/push release type. More than one button may be depressed to provide 'mixed trigger'.

The group of four lever switches defines the trigger signal and mode, i.e., internal or external, ac or dc coupled, positive or negative and AUTO or NORMAL. When all the switches are in the up position, a trace will always be triggered if the X V/DIV switch is set to S and a sweep velocity has been selected. The trace may not be visible if the shift controls are incorrectly set.

LEVEL

This potentiometer selects the point on the triggering waveform at which the trigger pulse is generated. The control is intended primarily to ensure that the timebase triggers consistently from the incoming signal and is not triggered by noise. The control remains effective in the AUTO mode.

V/DIV

This dual purpose control is similar to the Y channel V/DIV controls but it does not have the x 10 pull-out switch. Set the switch to S when using internal sweep. The S position replaces the 50V/div sensitivity range.

EXT

This BNC socket provides the connection for an external trigger signal.

CAL 60mV

This 4mm socket provides an output comprising an accurately defined 60mV positive-going edge which always appears near to the centre of the displayed trace.

Z MOD

This BNC socket provides the connection for the Z (brilliance) modulation input signal.

This combined screw terminal and 4mm socket provides a front panel earth point. It is connected directly to chassis.

EXT X

This BNC socket provides the connection for an external horizontal deflection signal input.

3.1.3 Rear Panel

Standard P.O. 2-pole jack sockets are provided on the rear panel for a FOOTSWITCH which performs the same function as the front mounted RECORD button. An audio output and an auxiliary a.c. power outlet are also provided. In addition, supply fuses are fitted to the rear panel in the area where the captive lead enters. A 3-way DIN socket on the rear plate of the module carries ±12V regulated supplies for use with external pre-amplifiers.

3.2 Installation

3.2.1 Introduction

3.2.1.1 When the instrument is received, it should be unpacked and examined for any superficial damage which may have occurred in transit. The supplier should be notified of any such damage forthwith.

3.2.1.2 The line voltage selector switches, situated on the rear panel of the instrument, should be set to the voltage nearest to the nominal a.c. line voltage. If the nominal voltage is between two selector values, use the higher setting.

3.2.1.3 Connect a suitable plug to the power lead using the colour code brown = line, blue = neutral and green/yellow = earth. If the local supply has no earth, connect the 'safety earth' terminal on the rear of the instrument to a known and tested earth. Failure to earth the instrument adequately is prejudicial to both safety and performance.

3.2.2 First Time Operation

3.2.2.1 Before switching on the FOR-4.2 for the first time, set the front panel controls as follows:-

Y1, Y2, Y3, Y4 (shifts)	mid-range, all beams turned ON
X SHIFT	mid-range, x 10 expansion OFF
BRILLIANCE (display)	maximum counter-clockwise
FOCUS (display)	mid-range
AUDIO	maximum counter-clockwise
GRAT	maximum counter-clockwise
BRILLIANCE (recorder)	maximum counter-clockwise
MODE	SS
SPEED	5cm/sec
SWEEP VELOCITY	100ms/div
Y1, Y2, Y3, Y4 (audio)	all out
TRIGGER switches, i.e., INT, AC, +VE, AUTO	up

3.2.2.2 Connect the instrument to the a.c. power using the power lead. Press the POWER push-button and note that the adjacent warning light is illuminated. The instrument requires approximately 30 seconds warm-up time before making any further adjustment.

3.2.2.3 Turn the BRILLIANCE (display) control clockwise until all four traces are clearly seen. Adjust the FOCUS (display) for best definition. Position the four traces using Y1, Y2, Y3, Y4 and X SHIFTS. Observe that the sweep speed changes as the SWEEP VELOCITY push-buttons are pressed. Advance the GRAT control clockwise to illuminate the engraved scales on the graticule.

3.2.2.4 The recorder camera is hinged at the lower edge and held by a spring clip at the top edge. Pull on the top edge of the camera and lower it forward out of the front panel. Select the SUP mode and operate the RECORD switch upwards. Adjust the record BRILLIANCE control to obtain a bright, clear display on the record CRT. The FOCUS control in the top right-hand corner of the recess from which the camera was withdrawn; it should be adjusted for optimum trace clarity The trace may be viewed directly along the axis of the CRT, as oblique viewing will give trace distortion. After the traces have been set up, release the RECORD switch and verify that the trace disappears. Select each record mode in turn and operate the RECORD switch; verify that the resultant record conditions correspond to the selected mode.

3.2.2.5 Connect a suitable signal to the Y1 input. Press the Y1 audio select push-button and turn the AUDIO volume control clockwise. Verify that the signal on Y1 is heard through the loudspeaker.

3.3 Operating Notes

3.3.1 Vertical Deflection Amplifiers

3.3.1.1 The four vertical deflection amplifiers have identical circuits. The inputs are connected through BNC sockets and the input impedance to each channel will match a standard passive oscilloscope probe. When connecting the inputs to the four amplifiers, take care to avoid multiple earthing which would cause earth loop currents and introduce unwanted noise signals.

3.3.1.2 The input signal coupling is selected by a 3-position switch. DC coupling is required for very low frequency signals and for measurement of d.c. levels. AC coupling is suitable for signals between 1·6Hz and 125kHz and is essential when the signal to be measured is superimposed on a large d.c. signal.

3.3.1.3 The input earthed position grounds the amplifier input and open circuits the input socket. This facility is useful in determining the earth reference level when measuring d.c. coupled signals.

3.3.1.4 The input sensitivity for each channel is selected by a 12-position switch. To check the sensitivity, select d.c. coupling and connect the amplifier input to the CAL60mV output socket. Set the V/DIV switch to 0·01 (10mV/div) and verify that the displayed signal fills six vertical graticule divisions. If necessary, the sensitivity can be adjusted by the internal preset gain control.

3.3.1.5 If a passive probe is being used for connection to the signal, first connect the probe output to the amplifier input and the probe input to the CAL 60mV output. Set the probe to x 10 and, using a screwdriver, adjust the probe compensating capacitor (built into the probe) until the displayed amplitude calibration waveform is free from droop and overshoot.

3.3.2 Timebase Trigger

3.3.2.1 To trigger the timebase from one of the displayed signals, first select the required trigger source by means of the group of four push-buttons. On the group of three push-buttons, select INT. together with the required polarity and coupling (a.c. or d.c.). Turn the TRIGGER LEVEL control clockwise until stable triggering is obtained. If satisfactory triggering cannot be obtained, increase the sensitivity of the relevant channel to obtain a larger triggering signal. Normally, use only one displayed signal as the trigger source at any one time. The timebase may be set to free-run if required.

3.3.2.2 To trigger the timebase from an external signal, select EXT, together with the required polarity and coupling (a.c. or d.c.). Connect the external trigger signal to the EXT TRIG input socket. Adjust the TRIGGER LEVEL control until the timebase triggers satisfactorily.

3.3.3 X-Y Display

3.3.3.1 The horizontal deflection amplifier is similar to the vertical deflection amplifier, but has only eleven sensitivity ranges. The amplifier can be calibrated by the method described for the vertical deflection amplifiers. The horizontal deflection signal is connected to the EXT X socket and, as soon as a sensitivity range is selected, the internal timebase is switched off. Thus, a true X-Y display can be obtained.

3.3.4 Z Modulation

3.3.4.1 Internally generated brilliance modulation signals are used to brighten the trace during the sweep and blank it during beam switching. However, when the internal timebase is not in use, external brilliance modulation signals are desirable to brighten the trace when required. These external Z modulation signals are connected to the Z MOD input socket. The input is d.c. coupled and, at the correct brilliance level, a signal of 1V or 2V (pk-pk) will give optimum grey scale.

3.3.5 Fibre-Optic Recording

3.3.5.1 Four recording modes are provided: single shot, superimposed, raster and continuous. These may be used with internal sweep or external horizontal deflection to give six meaningful modes of operation.

3.3.5.2 The single shot mode (SS) with internal timebase is obtained by pressing the SS button. A record will be obtained by operating the RECORD switch or the FOOTSWITCH (if fitted). The first complete trace after the RECORD switch has been operated will be recorded. The paper will then automatically advance and await the next record command. The record command is remembered by the logic and the switch need be pressed down only momentarily. This mode is useful for recording very low speed transient phenomena; the FOR-4.2 fulfils the function of a storage oscilloscope but produces a permanent record.

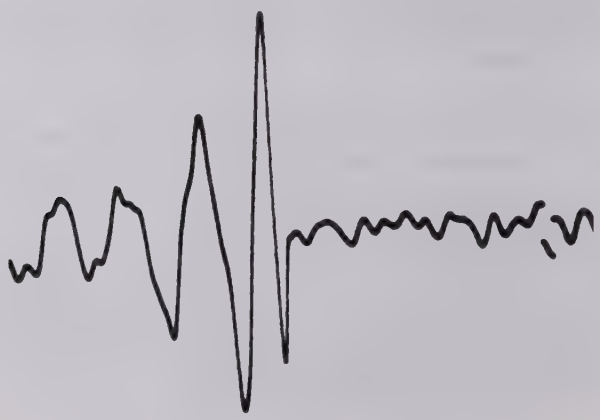


Fig. 3.2 Single Shot

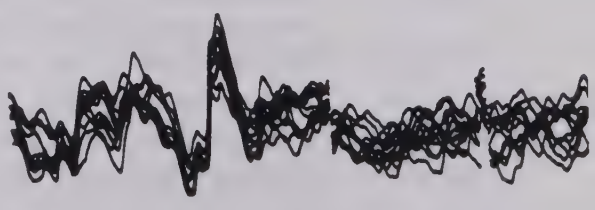


Fig. 3.3 Superimposed

3.3.5.3 The superimposed (SUP) mode with internal timebase is obtained by pressing the SUP button. A record will be obtained by setting the RECORD switch upwards or operating the FOOTSWITCH (if fitted). The record will commence with the first complete trace after the RECORD switch is operated and all traces thereafter will be recorded, superimposed, until the RECORD switch is released. The paper will then advance and await the next record command. The traces are recorded on stationary paper, superimposed one on the other. Thus, average values may be investigated and changes of level noted.

3.3.5.4 The raster mode (RASTER) with internal timebase is obtained by pressing the RASTER button. A record will be obtained by setting the RECORD switch upwards or operating the FOOTSWITCH (if fitted). The record will commence with the first complete trace after the RECORD switch is operated and all traces thereafter will be recorded until the RECORD switch is released. The traces are recorded on moving paper forming a 'raster' of traces. The paper will continue to move when the RECORD switch is released until the record is clear of the CRT face. The raster of traces clearly shows any significant trends in the recorded signal. The selected paper speed should be compatible with sweep speed and repetition rate to obtain satisfactory recordings with minimum slope due to record movement. This mode provides high time resolution with minimum paper consumption. Table 3.1 lists paper speeds for various trace spacings and timebase velocities. The information given assumes that the sweep repetition rate is the maximum available for the specified sweep velocity. Using slower triggering rates, wider separations are obtained. For satisfactory operation in the raster mode, select the timebase speed which produces the required time resolution, then determine the most suitable sweep spacing and select the relevant paper speed. Use the smallest acceptable vertical deflection so that spacing may be minimised to limit display skew and achieve maximum paper economy.

TABLE 3.1

Sweep Speed	1mm	2mm	5mm	10mm	20mm	50mm Sweep Spacings
0·05ms/div						
0·1ms/div	100cm					
0·2ms/div	50cm	100cm				
0·5ms/div	20cm	(40)cm	100cm			
1ms/div	10cm	20cm	50cm	100cm		
2ms/div	5cm	10cm	(25)cm	50cm	100cm	
5ms/div	2cm	(4)cm	10cm	20cm	(40)cm	100cm
10ms/div	1cm	2cm	5cm	10cm	20cm	50cm
20ms/div	0·5cm	1cm	(2·5)cm	5cm	10cm	(25)cm
50ms/div	2mm	(0·4)cm	1cm	2cm	(4)cm	10cm
100ms/div	1mm	2mm	0·5cm	1cm	2cm	5cm
200ms/div	0·5mm	1mm	(2·5)mm	0·5cm	1cm	(2·5)cm
500ms/div	0·2mm	(0·4)mm	1mm	2mm	(0·4)cm	1cm

Note: The body of the table lists paper travel per second. Figures in parenthesis are not available on the push-buttons and the nearest standard speed should be used. Paper speeds below 0·5cm/s are only available on FOR-4.2's fitted with 'divide by 10' or 'divide by 50' facilities.

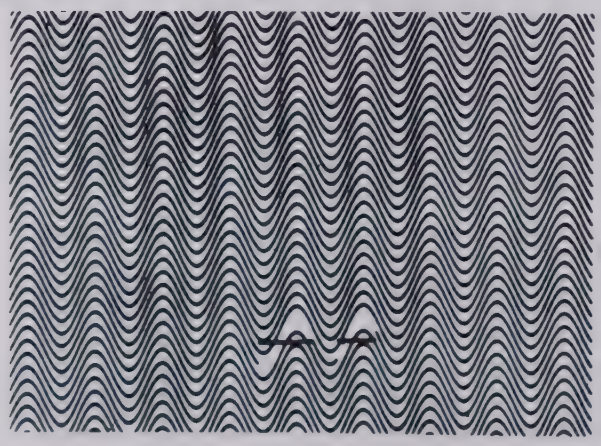


Fig. 3.4 Raster

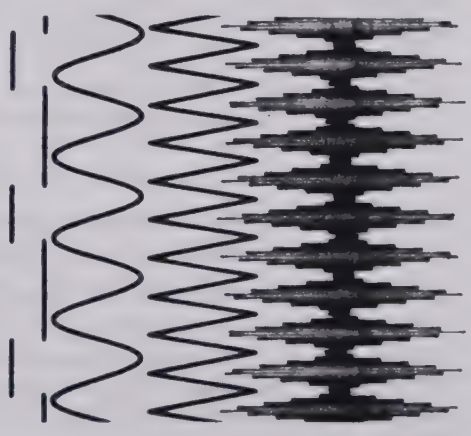


Fig. 3.5 Continuous

3.3.5.5 The continuous mode (CONT) is obtained by pressing the CONT button. In this mode, the internal sweep is not used. The vertical deflection signals are switched from the Y plates to the X plates of the CRT and the record is made on moving paper. In this way, a plot of signal against time is provided, the timescale being determined by the rate of paper movement. Recording will commence when the RECORD switch or the FOOTSWITCH is operated and will continue until the switch is released. In this mode, the FOR-4.2 may be considered as a high speed, 4-channel UV recorder.

3.3.5.6 The single shot (SS) and superimposed (SUP) modes with external X deflection give true X-Y plotting on stationary paper. The X deflection signal is connected to the EXT X socket and the V/DIV switch is set to give the required X sensitivity. With the EXT/MAN switch set to MAN, recording will commence when the RECORD switch is operated and will continue until it is released.

Fig. 3.6 X-Y Plotting

3.3.5.7 When EXT is selected, a +12V signal on the EXT GATE socket executes the camera and + GATE functions. The record circuit is primed by operating the RECORD switch or the FOOTSWITCH and the EXT GATE signal will then initiate a record cycle. In the SS mode and the SUP mode, a record cycle is initiated by the start of the EXT GATE signal and will continue until the EXT GATE signal is removed. The SUP mode has particular applications in recording the outputs from analogue hybrid computers solving iterative and boundary problems.

3.3.5.8 When working without internal sweep, a brightened trace may be obtained to facilitate adjustments by selecting MAN and operating the RECORD switch. A steady bright-up is obtained which may be cancelled by releasing the RECORD switch. Care must be taken not to over-brighten a static display or the tube phosphor may be damaged.

3.3.5.9 The SPACE button is provided for running paper out of the camera. The button is press lock/press release. When the button is locked in, the paper will run on by one tube height whenever the mode is changed from CONT or RASTER to any other mode. In addition, the paper will run on by one tube height whenever the button is released.

3.3.5.10 The graticule on the monitor CRT is engraved with dotted lines to indicate the limits of recording area on the fibre-optic tube. Any display which appears outside the limits of the graticule will not be recorded.

3.3.6 The Recording Unit (Paper Loading)

3.3.6.1 The rolls of paper are supplied in separate packs which may be opened in normal daylight although bright sunlight should be avoided. The spool is placed in the paper box at the rear of the cassette, against the flap, with the free end of the spool coming upward so that the emulsion (faintly coloured) side is presented to the face of the CRT. The free end of the paper is then placed, emulsion side outwards, between the rubber capstan roller and the white nylon pinch roller. Pull the belt drive towards the operator until the paper end appears at the front aperture of the recording unit.

3.3.6.2 The recording unit should then be pushed back into place slowly, at the same time pulling the paper smoothly through the slot to take up the slack paper. With the unit in place, the recorder is ready for use. At 100cm/s paper speed, a roll lasts 30s. When the end of the roll is reached, the unit may be hinged down and a new roll of paper inserted after removing the spent core.

3.3.6.3 When used with the take-up facilities to produce darkroom processed records, the following procedure should be adopted:-

Load the paper as already described. This will leave a leader of paper approximately 10cm long protruding from the recording unit. Thread this paper through the slot in the faceplate of the take-up cassette and fix the faceplate to the front of the recording unit. Cut or tear the corners of the leading edge of the paper to produce a tongue. Feed this tongue into the slot in the take-up spool. Wind the loose paper onto the spool, emulsion side inwards. Fit the spool into the slots provided in the wings of the faceplate. Fit the spring belt over the pulley at the end of the spool without twisting the belt. Briefly run the recording unit motor slowly to verify that the paper is running smoothly and is winding evenly onto the take-up spool.

Fix the cover onto the take-up cassette.

When recording is completed, remove the belt from the spool pulley. Lift off the take-up cassette and tear the recording paper along the top edge of the recording unit. Open the cassette in a darkroom by pressing down on the flaps on the top and bottom of the case and withdrawing the mounting plate complete with spool.

3.3.6.4 Paper Characteristics

The recording paper (e.g., Kodak 1895) is developed (i.e., exposed to ambient light) and the image appears rapidly. For protection, if prolonged exposure to strong light is expected, an aerosol spray may be used (Kodak aerosol lacquer for protecting UV records).

Alternatively, if Kodak 1801 is used with full chemical processing, an enhanced contrast is achieved with archival permanence. A take-up cassette is therefore available. This paper may also be photo-developed and subsequently chemically processed if long term stability is needed.

4.0 CIRCUIT DESCRIPTION

The operation of the FOR-4.2 is explained using block diagram C3/12316. In the following section, is will been seen that the explanation of the deflection amplifiers refers to a circuit diagram incorporated in the text, and not to the display circuit diagram. This is because the deflection amplifier is common to both display and camera control boards in the DFO6M.

4.1 Main Display Board (see Circuit Diagram C/12446/1 and Sweep Velocity p.c.b. circuit C/12448/1)

The main display board contains a number of circuits. They are as follows:-

Sweep Generator
Beam Switch
Deflection Amplifiers
A3 Stabiliser
+5V Stabiliser
Audio Summing Amplifier
Amplitude Calibration Generator

4.1.1 Sweep Generator

4.1.1.1 Introduction

Sweep velocity is selected by interlocked push-buttons. Intermediate values are selected by operating more than one push-button simultaneously and adding the selected sweep velocities. An independent push-button at the end of the switch bank switches between the two ranges shown.

The sweep is generated by a current source charging a capacitor which is then discharged by a transistor switch. The sweep will either run continuously, or may be triggered from the Y input signals or from an external trigger signal.

4.1.1.2 Principle of Operation and Circuit Description

Sweep capacitors are mounted on the sweep velocity board and these are connected from the junction of R97 and R98 to +12V. Q38 passes a constant current, determined by the sweep velocity resistors on the sweep velocity board. When the sweep begins, the sweep capacitor charges negatively until Q40 conducts, i.e., when the emitter becomes forward biased with respect to the base, the potential of which is fixed by the chain R100, R104 and R105. If Q38 supplies a current I, the rate of change of voltage $\frac{dv}{dt}$ equals $\frac{I}{C}$ volts/second where C is the sweep capacitor.

4.1.1.3 By making the voltage across the sweep resistor equal to the sweep amplitude at the gate of Q43, the sweep duration can be made equal to CR. The sweep velocity resistors are normally short circuited by their switches; when a switch is operated, the relevant resistor is added to the circuit. With no buttons pressed, the charging current is limited by R98.

4.1.1.4 At the end of the sweep, Q39 and Q40 switch on, switching off Q37 which in turn, cuts off Q38 to stop the constant charging current. R94 ensures that Q38 switches off. The switching threshold is set up by RV3 to calibrate the sweep velocity. If Q41 is turned off)+12V on T.B Control), then Q39 and Q40 will be held conducting through D15 and R99, inhibiting the sweep. A new

sweep can be initiated by monentarily turning on Q41 which enables Q39 and Q40 to switch off. C14 is a speed-up capacitor for Q37. C15 ensures that Q39 switches off during a trigger pulse.

4.1.1.5 Q43 is the output buffer stage of the sweep generator; it draws current from the junction of R107, R108. These are connected between +240V and +12V and give a source potential of approximately +22V, to permit adequate linear signal excursion. R110 and RV4 set the mean potential of the sweep to a d.c. level of +6V at the emitter of Q45.

4.1.1.6 Q48, Q50 and Q51 form an inverting amplifier with a gain of x 1 or x 10 as selected by the FET switch Q49. In the x 1 mode, the gain is determined by the feedback resistor R121; Q49 is conducting and short circuits R118. In the x 10 mode, Q49 is cut off and R118 is added to the feedback resistor, increasing the amplifier gain by ten times; also, Q52 is switched on and draws current through R117 and R127 from the base of Q48; R127 is adjusted on test to obtain correct operating conditions. In both modes, this amplifier shifts the mean d.c. level of the sweep to -6V.

4.1.1.7 Positive gate is taken from the collector of Q37 via R90 and D6. R90 provides short circuit protection while D6 ensures that external circuits generating negative signals on the positive gate line will not affect Q37 (i.e., the unit only requires 0 to +12V for + GATE).

4.1.2 Beam Switch Generator

4.1.2.1 Introduction

The Y deflection signal is a composite waveform made up of the four Y inputs; these inputs are coupled, in turn, to the beam switch summing amplifier by gating the transistors. The spot is blanked off during beam switching to allow the gating circuit and deflection amplifier to settle. A brighter trace may be obtained if only one of the two beams is required. Y3 and Y4 will be extinguished if the Y4 shift control is turned fully counter-clockwise. Y1 and Y2 will be selected at twice the normal rate, doubling the brilliance. Y1 only will be displayed if the Y2 shift potentiometer is turned fully counter-clockwise. Y1 will then be displayed at four times the normal rate, giving a further increase of brilliance. The Y inputs are fed via a unity gain buffer with 100kΩ input impedance.

4.1.2.2 Circuit Description

The circuit will be broken down for descriptive purposes into the following elements:-
Square Wave Oscillator and Buffer
Twisted Ring Counter
Beam Switch Buffer Amplifiers
Beam Switch Summing Amplifier

4.1.2.2.1 Square Wave Oscillator and Buffer

The oscillator comprising Q22 and Q23 produces a square wave at Q23 collector. R54 and R55 are connected from base to collector instead of to the more usual +5V, eliminating the risk of a lock-out condition with both transistors saturated. Q25 is a buffer inverter which generates a positive clock pulse from the negative-going edge of the output waveform.

4.1.2.2.2 Twisted Ring Counter

If the reader is unfamiliar with logic circuits, he should refer to Appendix A1 before proceeding further with this explanation.

The twisted ring counter can be gated to operate in three modes, as follows:-

i) Divide by 4 with gates (Y1, Y2 only) and (Y1 only) low

ii) Divide by 2 with gates (Y1, Y2 only) high and (Y1 only) low

iii) Single beam with gates (Y1, Y2 only) and (Y1 only) high.

For a 4-beam display, SW30 and SW40 are closed (see Fig. 4.1) - Y2 and Y4 shifts not fully counter-clockwise - and the (Y1, Y2 only) and (Y1 only) gate lines are low. Gate 3 will, therefore, have a high output and Gates 1 and 2 will act as inverters for B and $\overline{B}$.

Assume that, after n clock pulses, the outputs A and B are high (see Truth Table of Fig. 4.2). After each clock pulse, B will have the previous value of A and A will have the complement of the previous value of B. The counter will cycle through all four possible combinations and R154 to R161 will select one of the transistors Q68 to Q71 which turn off when low outputs appear on a pair of base resistors.

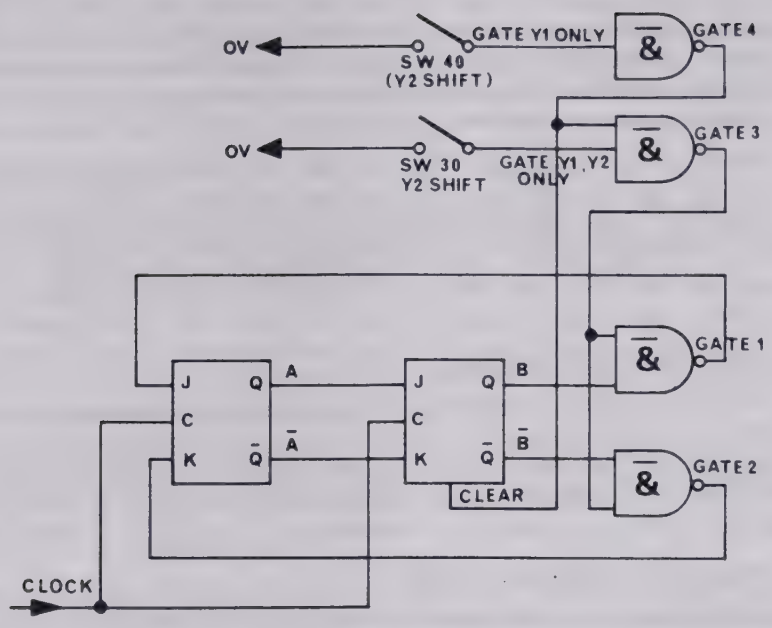
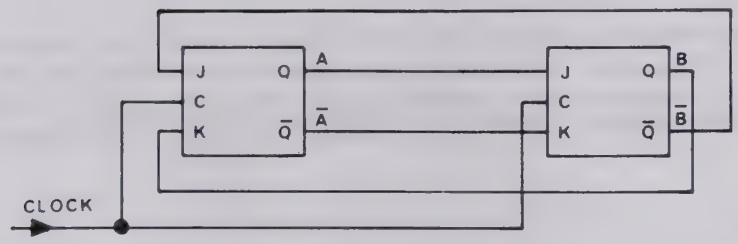


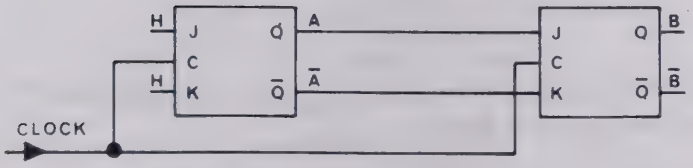
Fig. 4.1 Twisted Ring Counter



TRUTH TABLE

t	A	B	Y
N	H	H	4
N + 1	L	H	2
N + 2	L	L	3
N + 3	H	L	1
N + 4	H	H	4

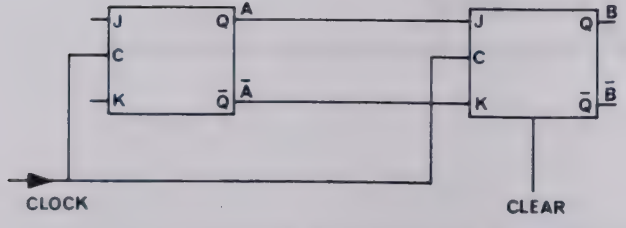
Fig. 4.2 Simplified Counter for producing Four Beams



TRUTH TABLE

t	A	B	Y
N	H	L	1
N + 1	L	H	2
N + 2	H	L	1

Fig. 4.3 Simplified Counter for producing Two Beams



TRUTH TABLE

t	A	B	CLEAR	Y
n	H	L	L	1
n+1	H	L	L	1
n+2	H	L	L	1

Fig. 4.4 Simplified Counter for producing Single Beam

For a 2-beam display, SW30 is open (Y4 shift fully counter-clockwise) and SW40 is closed, setting (Y1, Y2 only) gate high and (Y1 only) gate low. Gate 3 will have a low output and Gates 1 and 2 will, therefore, give high outputs to J and K of the first bistable. The equivalent logic diagram is shown in Fig. 4.3. The first bistable will complement with each clock pulse and the second bistable will have outputs which are the complements of the first bistable. Y1 and Y2 only are displayed and the truth table (see Fig. 4.3) is much simplified. Q68 and Q69 are the only transistors which receive the required combination of low signals on their base resistors.

For single beam operation, SW30 and SW40 are open (Y2 and Y4 shifts fully counter-clockwise) and the (Y1, Y2 only) and (Y1 only) gate lines are high. The output of Gate 4, therefore, goes low and the output of Gate 3 goes high. The low signal on the clear line of the second bistable holds that bistable with B low. This gives a high on the J input and a low on the K input, so that A is high. This gives two low signals to the base resistors of Q68 and the Y1 signal is permanently connected to the deflection amplifier.

4.1.2.2.3 Beam Switch Buffer Amplifiers

Four identical amplifiers are used; of these, only the amplifier for signal Y1 will be considered. The Y1 input from the amplifier module is connected to Y1 SIG. The input resistance is R131, which supplies the base current of Q60 when the input is open circuited. Q60 and Q64 form a high input resistance unity gain buffer amplifier isolating the signal line from the beam switch. R143 determines the gain of the buffer amplifier.

4.1.2.2.4 Beam Switch Summing Amplifier

R142 introduces the shift current (see Fig. 4.5). The transistor switches Q68 to Q71 are represented by SW1-4 and are normally closed; they are opened, in turn, by the twisted ring counter. When a switch is opened, its associated diode conducts and the sum of the currents from the signal and shift flows into the summing amplifier input. An antiphase signal will appear at the output. SW1-4 are fed from A, $\bar{A}$, B and $\bar{B}$ of the twisted ring counter. Q68 (SW1), for example, is fed from $\bar{A}$ and $\bar{B}$; it will be switched off when both these outputs are low.

The summing amplifier comprises Q72 and Q73. Q72 is used in common base and its main purpose is to define the d.c. level of the input. It transfers the input current to the base of Q73 but provides no current gain to the amplifier. R168 provides negative feedback to Q72, making the emitter a summing junction. The output voltage at Q73 collector for a trace at the centre of the screen is approximately −5·7V.

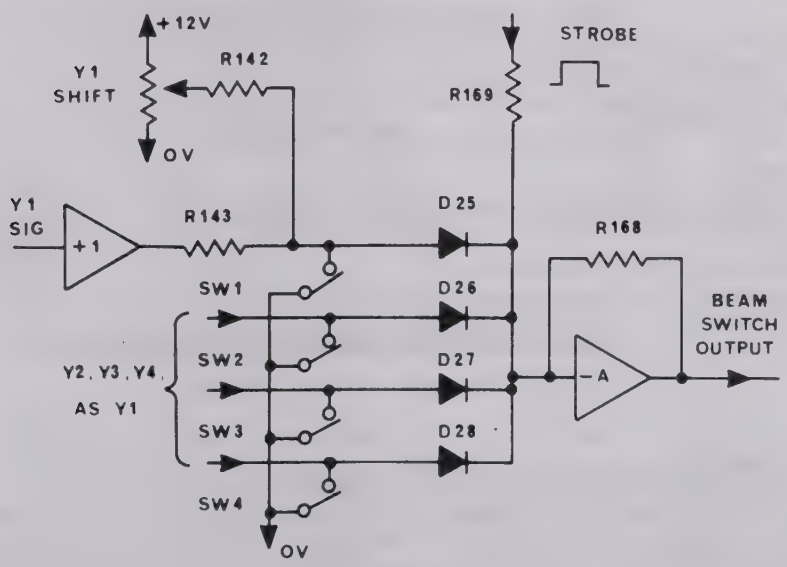


Fig. 4.5 Simplified Circuit Diagram of Beam Switch Summing Amplifier

4.1.3 Deflection Amplifier

4.1.3.1 Introduction

There are four similar deflection amplifiers used in the instrument to drive the X and Y plates of the display and the recording cathode ray tubes respectively. The circuit configuration used gives a push-pull output with a high slew rate and excellent supply ripple rejection. In addition, the large amount of negative feedback inherent in the design ensures very good d.c. and gain stability.

4.1.3.2 Circuit Description (see Fig.4.6)

Two NPN/PNP transistor pairs Q1, Q2 and Q4, Q5 provide the gain elements of the push-pull amplifier - each pair can be considered as a high performance compound transistor. The push-pull output is obtained by driving Q4, Q5 through the inverter Q3.

The voltage at the base of Q3 will cause a change in its emitter current equal and opposite to the change of current in R4. The collector current of Q3, approximately equal to its emitter current, will cause a voltage at the collector of Q5 which is in phase with the input. The gain of each element - Q1, Q2 and Q4, Q5 - is established by the ratios R3/R4 and R9/R10.

As the input impedance is relatively well defined as R4 in parallel with R5, the gain of the amplifier can be varied by the single series resistor RV1. When RV1 = 0, gain = R3/R4 = approximately 22.

When RV1 = 10kΩ, gain = $\frac{R3/R4}{1 + RV1/RA}$ = approximately 5·8 where RA = R4 in parallel with R5.

The mean plate potential (M.P.P.) is adjusted by RV2 which supplies equal currents to the bases of Q2 and Q4 through R6 and R7. When RV2 is adjusted, the outputs will move together in phase to the change in potential at the wiper of RV2. The range of adjustments is ±12V x R3/R6 which is approximately equal to ±40V relative to the mean value of +120V.

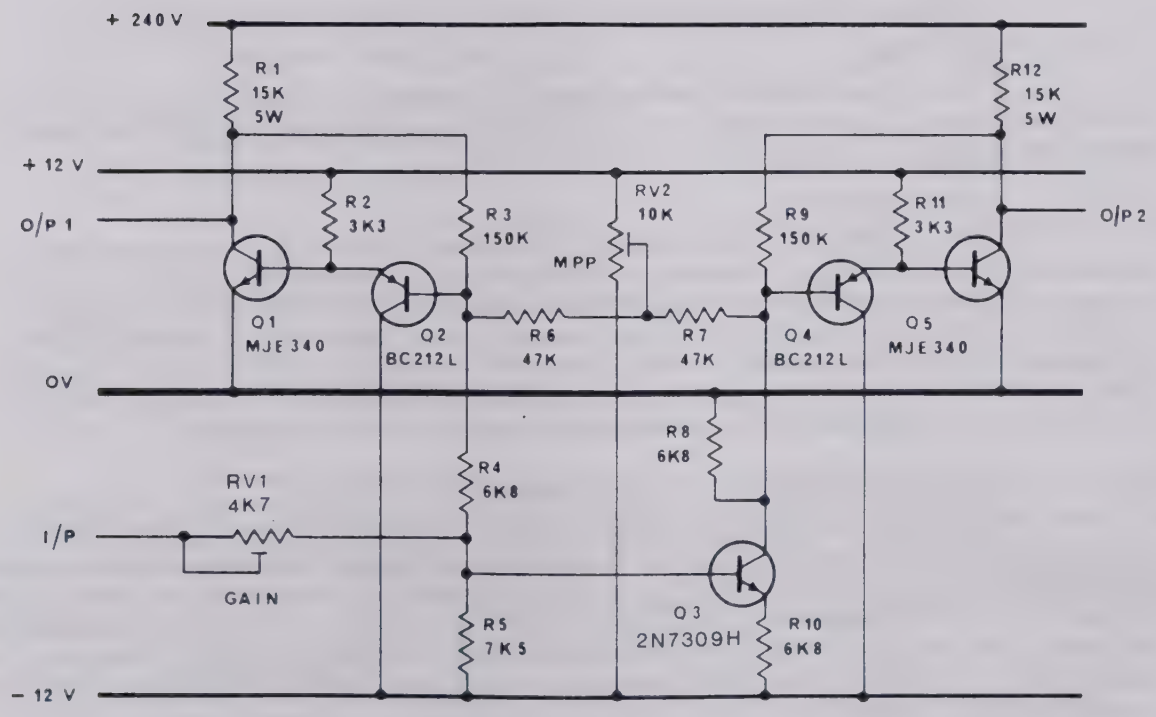


Fig.4.6 Deflection Amplifier Circuit

4.1.4 A3 Stabiliser

The first and third anodes of the CRT's must be approximately the same voltage as the mean of the deflection plates. As the deflection plates have variable mean plate potential (M.P.P.), A3 can be fixed using one stabiliser for both CRT's.

The M.P.P. of the deflection amplifiers is dependent upon the −12V and is independent of the unstabilised +240V. The A3 stabiliser is an emitter follower Q91; its base potential is determined by the high voltage zener diode D29. The A3 potential, taken from the emitter of Q91, will be approximately +120V.

4.1.5 +5V Supply Stabiliser

Q19 and Q20 form a complementary emitter follower which derives +5V from the +12V supplies for digital IC's. The voltage is determined by R45 and R46. R47 limits the current and the dissipation of Q20 in the event of a short circuit across the +5V. Crowbar protection is given by zener diode D4 which conducts only if the regulator operates incorrectly, limiting the +5V to a maximum of 6·8V.

4.1.6 Audio Summing Amplifier

4.1.6.1 Introduction

The amplifier is used to sum the Y signal inputs, as selected by the AUDIO push-buttons, and feed the resultant signal to the AUDIO GAIN control.

4.1.6.2 Circuit Description

The beam switch buffer amplifiers are used to avoid loading of the Y signal line by the audio amplifier. The outputs are fed via R130, R132, R134 and R136 to the AUDIO push-buttons. The Y signals selected are a.c. coupled via C22 to the base of Q74. R177 and C23 determine the amplifier gain and high frequency cut-off (15kHz). The d.c. conditions of the amplifier are set by R175 and R176 to give a quiescent output voltage of about 7V; C25 decouples noise from the −12V supply. C24 feeds to the front panel AUDIO GAIN control.

4.1.7 Amplitude Calibration Generator

4.1.7.1 Introduction

The amplitude calibration generator output is connected to a socket on the front panel of the amplifier module. It may be connected to any of the four amplifier channels to enable the sensitivity of the channel to be set accurately.

4.1.7.2 Circuit Description

Q75 and Q76 form a Schmitt trigger which changes state when the X output is at −6V. Because both transistors turn ON, the output is a fast negative-going excursion which occurs when the trace is approximately at the centre of the screen. The circuit resets during the flyback period. The Schmitt waveform from the junction of R191, R192 in the collector of Q76 is buffered by the inverting amplifier Q92 and fed to an attenuator consisting of R190, R193, R194 and the A.O.T. resistors R207, R208. R207, R208 are selected on test to give a signal amplitude of 60mV at the base of Q93, an emitter follower giving a low output impedance. R193 sets the reference level of the signal to be zero.

4.2 Sweep Velocity Board (see Circuit Diagram C/12448/1)

This board, mounted directly beneath the display CRT, operates in conjunction with the front panel push-button switches SW4/1a to SW4/8a. Seven of these switches are connected across the seven sweep velocity resistors. The resistors are shorted out when the push-buttons are relaxed and each resistor is connected into circuit when its associated button is pressed. When two or more buttons are pressed simultaneously, the actual sweep velocity is the sum of the velocities indicated by the pressed buttons. The low end of the resistor chain is connected to a front panel potentiometer which varies the current through the resistors to give fine control of velocity from x 1 to x 2·5.

The eighth push-button selects the timing capacitor, dividing the sweep velocity by one-hundred when the button is pressed.

A transistor is also fitted on this board to provide control of graticule illumination. The graticule lamps are connected in the emitter circuit of the transistor, while its base potential is adjusted by the GRAT control.

4.3 Focus and Brilliance Boards (see Circuit Diagrams C2/13505/1 and C2/13500/1)

4.3.1 Introduction

The instrument contains two of these boards, one for the display cathode ray tube and one for the fibre-optic recording tube. The boards are similar in operation but have minor differences. These boards supply the correct potentials to the cathodes, grids and focussing electrodes of the tubes and provide the required bright-up signals.

4.3.2 Circuit Description

The d.c. level from the front panel BRILLIANCE control is summed with the Z modulation signal and fed to the unity gain inverter Q1. The collector signal of Q1 provides the base potential for Q2, determining the bright-up signal amplitude. The emitter current of Q2 is divided between Q3 and Q4 and, when both of these are cut off, the collector of Q2 will go high, giving maximum brilliance on the CRT. When Q3 is gated on by the beam switch oscillator or Q4 is gated by the bright-up gate, the collector of Q2 will go low, blanking the CRT. The bright-up signal is a.c. coupled by C2 to the CRT grid, d.c. restoration being provided to -2kV by D1. The cathode potential is fixed by the zener diode D2, while R20, R21, RV1, R22 and D2 provide a potential divider supplying the necessary potential for A2. On the camera focus and brilliance board, transistor Q5 is added. This is switched by the bright-up gate and inhibits Z modulation signals during the blanking period.

4.4 Camera Control Board (see Circuit Diagram C/12447/1)

The camera control board contains circuits for:-

Producing a suitable camera blanking gate for each mode of filming to gate the bright-up signal on the camera focus/brilliance board.

Producing logic signals to gate the servo-controlled film/paper drive.

Switching beam switch to the horizontal tube axis for 'Continuous' recording.

Removing sweep for 'Continuous' recording.

The board also contains deflection amplifiers and part of the servo amplifier. For explanation of the deflection amplifiers, see 4.1.3.

The explanation of the servo amplifier is for the complete amplifier, although the output stage is situated in the camera.

If the reader is not familiar with the logic circuits in the following section, he should refer to Appendix A1.

4.4.1 Description of Camera Control System

4.4.1.1 Introduction

The system operation is described with the aid of the circuit block diagram (Drawing C5/11607). There are five modes of operation for recording and these are selected by means of four push-button switches on the front panel. They are identified from the top as 'Single Shot' (SS), 'Superimposed' (SUP), 'Raster' (RASTER) and 'Continuous' (CONT). A fifth push-button (SPACE) winds the film on by an additional half-frame after filming is completed in any of the selected modes to ensure the latest recording is clear of the camera cassette.

4.4.1.2 Single Shot Mode

4.4.1.2.1 Logic Sequence

When the SS push-button has been depressed, but the SPACE button has not, the following sequence of operation will take place when the FOOTSWITCH or RECORD button is operated:-

The FOOTSWITCH or RECORD button is connected to the input of a non-inverting buffer amplifier, A2, to eliminate the effect of contact bounce in the switch. The output of the buffer amplifier will change from high (+5V approximately) to low (0·6V approximately) and this will SET the bistable

comprising NAND-3 and NAND-4. The output of NAND-3 will now be high and the output of NAND-4 will be low. Thus, inputs J and K of bistable 1 (FF1) will be high and low respectively.

The circuit is now primed and awaits the next + GATE from the display board. This + GATE signal is inverted by amplifier A1 and provides a clock input to FF1 and FF2. The outputs of FF1 (Q and $\overline{Q}$) follow J and K to go high and low respectively. The outputs of FF2 do not change with the clock pulse as the outputs Q and $\overline{Q}$ are already set as J and K respectively.

Thus, with SS selected, $\overline{Q}$ of FF2 which is high provides one input to NAND-5. The second input to NAND-5, taken from Q of FF1, is high and the third input, + GATE, inverted by A1 and again inverted by NAND-1, is also high.

The output of NAND-5 is used to control two functions:-

a) Bright-Up:-
When NAND-5 received the positive gate, its output changed from high to low, thus operating NOR-3. The output of NOR-3 gates the bright-up signal to the camera CRT via the camera focus/brilliance board.

b) Motor Drive:-
The output of NAND-5 also provides one input to NAND-6, the second input being open circuit in this mode as SW2/2a (SUP) is open. When NAND-5 output goes low, NAND-6 toggles and its output goes high; this has no effect. When NAND-5 output returns to high after the bright-up has occurred, the negative-going edge at the output of NAND-6 provides a trigger pulse to the monostable SS2. The output from SS2, gated through NOR-4, drives the servo amplifier.

4.4.1.2.2 Reset of Logic

After the first positive gate has been used to drive the bright-up amplifier and camera control logic, the logic is ready to be reset.

The second positive gate will cause FF2 outputs to change state (FF1 will not change state with any further clock pulses applied until it has been reset).

When FF2 changes state, output $\overline{Q}$ changes from high to low. The input to NAND-5 through SW2/1a inhibits this gate to prevent any further positive gates from brightening up the CRT or triggering SS2.

The logic is reset by the output of a 3-input NAND-gate, NAND-2. When all three inputs are high, i.e., Q output of FF1 high, the footswitch released and the positive gate completed, the reset input of NAND-4 becomes low, causing the output of NAND-4 to become high. This puts a low to the 'clear' input of FF1 and the PRESET of FF2, instantly producing a low output on Q of FF1 ready for the next filming sequence to begin.

4.4.1.3 Superimposed Mode

4.4.1.3.1 Bright-Up

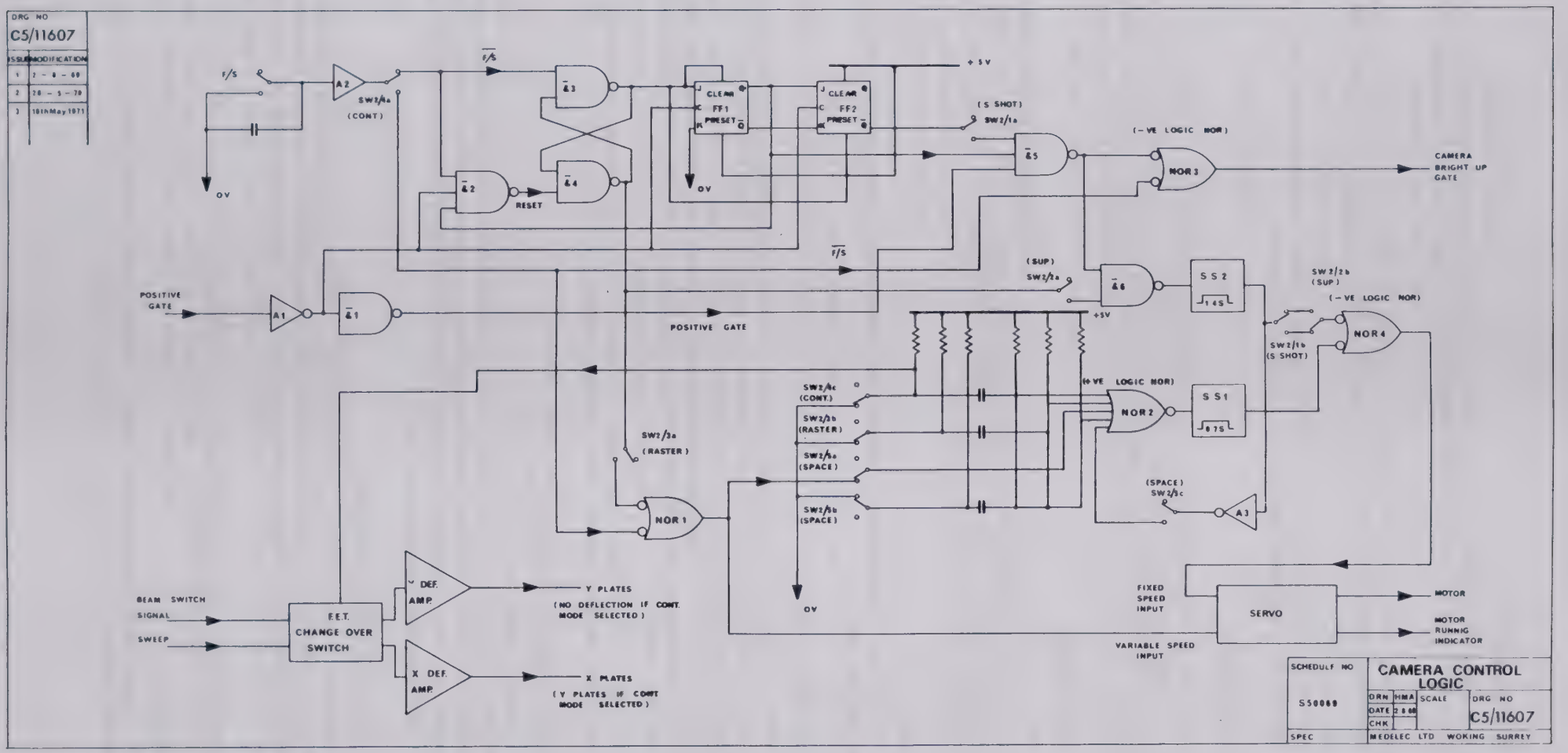
The conditions for bright-up in this mode are similar to those for the single shot mode, except that SW2/1a is not made and positive gates will not be inhibited while the footswitch is depressed. Reset is the same as for the single shot mode.

4.4.1.3.2 Servo Amplifier Drive

To prevent the monostable SS2 triggering at the end of the first positive gate, the output of NAND-6 is held high by the low input which is fed through SW2/2a from the output of NAND-4 (SW2/2a is made in this mode). This output is low because the bistable has been set. However, when the logic resets because the footswitch is no longer depressed, and conditions occur as described for the single shot mode, the output of NAND-4 becomes high. The final positive gate that brights up the CRT, gates NAND-6 and triggers SS2.

4.4.1.4 Raster Mode

The operation of the logic to produce a bright-up gate pulse is identical to that for the superimposed mode. When the footswitch is operated, the input to NOR-1 becomes low because SW2/3a is made. The output of this amplifier goes high, switching on the variable speed input to the servo amplifier. The output of SS2 is not required, so that SW2/2b and SW2/1b are opened. NOR-4 is still connected to SS1, should SPACE be required.


DRG NO
C5/11607
ISSUE MODIFICATION
1 2 - 8 - 69
2 28 - 5 - 70
3 18th May 1971
F/S
A2
SW1/4a
(CONT)
OV
RESET
&3
&4
&2
CLEAR
FF1
PRESET
FF2
+5V
(S SHOT)
SW2/1a
&5
(-VE LOGIC NOR)
NOR3
CAMERA BRIGHT UP GATE
(SUP)
SW2/2a
&6
SS2
1.4S
SW2/2b
(SUP)
(-VE LOGIC NOR)
NOR4
SW2/1b
(S SHOT)
POSITIVE GATE
A1
&1
POSITIVE GATE
+5V
SW2/4c
(CONT.)
SW2/3b
(RASTER)
SW2/5a
(SPACE)
SW2/5b
(SPACE)
(+VE LOGIC NOR)
NOR2
SS1
0.7S
SW2/3a
(RASTER)
NOR1
(SPACE)
SW2/5c
A3
BEAM SWITCH
SIGNAL
SWEEP
E.E.T.
CHANGE OVER
SWITCH
Y DEF.
AMP.
X DEF.
AMP.
Y PLATES
(NO DEFLECTION IF CONT. MODE SELECTED)
X PLATES
(Y PLATES IF CONT MODE SELECTED)
FIXED SPEED INPUT
VARIABLE SPEED INPUT
SERVO
MOTOR
MOTOR RUNNING INDICATOR
SCHEDULE NO
S50088
CAMERA CONTROL LOGIC
DRN HMA
SCALE
DRG NO
C5/11607
DATE 2.8.69
CHK
SPEC
MEDELEC LTD WOKING SURREY

4.4.1.5 Continuous Mode

With this mode selected, SW2/4a is made and the input to NAND-3 disconnected. When the output of A2 is low, the output of NOR-3 is high, applying bright-up for as long as the footswitch is depressed.

The output of A2 is also fed to NOR-1. The output of NOR-1 goes high when the footswitch is depressed. The output is again fed to the input of the servo amplifier which gives a variable speed drive to the motor.

The closure of SW2/4c activates the FET changeover switch which disconnects the Y deflection amplifier and connects the beam switch signal to the X deflection amplifier.

4.4.1.6 SUP/SS Mode

4.4.1.6.1 This mode is obtained when all the mode selection push-buttons are 'out'. It enables traces to be superimposed each time the footswitch or RECORD button is operated. No paper movement will occur unless the SPACE button is pressed or another mode is selected. When used in conjunction with a slow triggered timebase or an externally triggered sweep, superimposed single shots may be recorded.

4.4.1.6.2 Logic Sequence

SW2/2b and SW2/1b are both open in this mode and SS2 cannot therefore be triggered. Thus, there is no drive to the servo amplifier through NOR-4 and the paper does not move. With the SPACE button pressed, SS1 is triggered after each + GATE, through NAND-5, NAND-6 and SS2. This moves the paper by 4·3cm after each sweep while the footswitch is operated.

4.4.1.7 Space Mode

The film can be advanced one additional half-frame by one of three methods, independent of the recording mode selected.

4.4.1.7.1 Space Mode Lock-In

When 'single shot' or 'superimposed' modes are selected, the monostable SS2 will trigger to move the film on after recording has taken place. The output of SS2, after being inverted by A3, is fed to an input of NOR-2. This input becomes high and causes the output of this gate to become low. When the pulse produced by SS2 has ended, the negative-going edge fed from NOR-2 is used to trigger SS1. The output of SS1 drives NOR-4, whose output goes high when either of its inputs goes low, thus driving the constant speed input to the servo amplifier.

A similar operation occurs when 'raster' or 'continuous' modes are selected, except that the input to NOR-2 is derived from the output of NOR-1 through SW2/5a.

4.4.1.7.2 Space Selected Momentarily

In order to advance the film through the camera, the SPACE button may be depressed without locking-in. This produces a positive pulse on NOR-2, because of the capacitor and resistor network across the input of NOR-2 from SW2/5a. When the switch is made, the gate input is low; when it is not made, the input rises to a high state, thus producing a positive pulse on one of the inputs of NOR-2. SS1 will now trigger as for the other conditions for spacing the film.

4.4.1.7.3 Raster or Continuous Disconnected

If, after filming in 'raster' or 'continuous' mode, it is changed to 'single shot' or 'superimposed', the film will space on independently of the SPACE switch. This is accomplished by identical networks to those which were used to inch the film on as described for the 'space' modes, except that the pulse derived depends on either SW2/4c or SW2/3b (CONT or RASTER) being opened.

4.4.2 Description of Circuit Elements (Circuit Diagram C/12447/1)

4.4.2.1 Introduction

The camera control system circuit consists of different circuit functions constructed either by integrated or discrete component circuit techniques. They are as follows:-

Logic Amplifiers
Deflection Amplifiers
Positive Logic NAND gates
Positive Logic NOR gates
Negative Logic NOR gates
Single Shot Circuits (Monostables)
J. K. Bistables
+5V Supply Stabiliser
FET Changeover Switch
Servo Amplifier

4.4.2.2 Logic Amplifiers

4.4.2.2.1 Logic Amplifier A1

This amplifier (Q3) acts as a gating circuit and inverter. Q3 is normally cut off with its base held at 0V through R10. The positive gate pulse, coupled through R9 and zener D2, switches on Q3, producing a negative-going edge at the collector. This drives the clock inputs of the J-K bistables and an input of NAND-2 (M3b) and NAND-1 (M2d). The amplifier is inhibited by 0V on the 'XY GATE' input.

4.4.2.2.2 Logic Amplifier A2

This amplifier consisting of Q1, Q2 is designed to inhibit footswitch contact bounce appearing at the input to the logic. When the input through D1 goes to 0V, as the footswitch makes, the voltage across C1 decreases and Q1 turns on, thus turning Q2 on. Hysteresis is obtained by feedback via R5 giving noise immunity to the amplifier.

4.4.2.2.3 Logic Amplifier A3

This amplifier, Q12, inverts the output of SS2 (Q10 and Q11) so that the correct logic signal is available for the input to NOR-4 (D12 and Q13).

4.4.2.3 Deflection Amplifiers

A full description of the deflection amplifier is given for the display board (see 4.1.3.). It should be noted that two shift and gain potentiometers are fitted to the X deflection amplifier because it is used both for 'continuous' and 'superimposed' filming and because the sensitivity ratio of the CRT is not 1:1, giving different sensitivity for a Y signal displayed horizontally.

4.4.2.4 Positive Logic NAND Gates

NAND-1 to NAND-6 are integrated circuit positive logic NAND-gates. They are transistor transistor logic (TTL) gates incorporated in two packages, M2 and M3. Their function is described as follows:-

If all the inputs are high, the output is low; if one or more inputs are low, the output is high. If any gate input is left open circuit, it should be considered as a high input. C2 produces a delay to the reset of NAND-2 to ensure that FF1 settles into its new state before resetting.

4.4.2.5 Positive Logic NOR Gates

NOR-2 is a positive logic NOR gate consisting of Q13, D11-D15, etc. This gate determines the conditions for winding film on in the 'space' mode as described in 4.4.1.7. When SW2/5b opens, a positive pulse is produced as C5 charges through R25. When the switch closes, C5 discharges. A similar operation to the above occurs when SW2/3b and SW2/4b are opened. The other two inputs become positive when either A3 output or NOR-1 output becomes high.

When one of the inputs becomes high, the relevant diode conducts, thus producing a positive voltage on the base of Q13, causing it to turn off. Thus, the 'positive logic NOR' function is obtained when a high condition on any input causes the output to become low.

4.4.2.6 Negative Logic Logic NOR Gates

NOR-1, NOR-3 and NOR-4 are negative logic NOR gates, i.e. with any input low, the output will go high.

4.4.2.6.1 NOR-1

When SW2/4a is switched to CONT or SW2/3a is switched to RASTER, the base of Q5 will go low each time the footswitch is operated. The resultant high output switches on Q23 to start the servo motor. The subsequent low when the footswitch is released will be coupled through SW2/5a to NOR-2 if SPACE is selected.

4.4.2.6.2 NOR-3

When the output to either D5 or D6 becomes low, current is drawn through R26 and D7 is reverse biased; Q8 cuts off as its base is low. Therefore, the collector becomes high, giving the function 'negative logic NOR'. The output is used to gate the CRT bright-up on the camera focus and brilliance board after inversion by Q9.

4.4.2.6.3 NOR-4

When the input to either D19 or D20 goes low (SS2 or SS1 triggered), the diode is forward biased and Q16 switches on as its base is low. Therefore, the collector becomes high, giving the function 'negative logic NOR'. The output is used to switch on the servo motor at a fixed speed through Q26.

4.4.2.7 Single Shot Circuits

There are two monostable circuits, SS1 and SS2, and they are both collector coupled.

4.4.2.7.1 SS2

This circuit receives a negative-going pulse which, derived from the output of NAND-6, is differentiated by the network C6 and R35. The positive pulse is stopped by D8. Q11 is conducting in the stable state and Q10 is cut off. The negative trigger pulse turns off Q11 and Q10 turns on. C7 charges through the timing resistance and, after a time set by RV10, the circuit reverts to its original state. D10 prevents excessive reverse bias on the base of Q11. R39 provides noise immunity. R36 and D9 hold the base of Q11 positive to prevent false triggering from taking place.

4.4.2.7.2 SS1

SS1 triggers when a positive pulse appears on the base of Q14. This pulse is produced from the output of NOR-2; it is differentiated by C9 and R50 and negatively clipped by D16. When the pulse appears, Q14 turns on and has an astable period set by RV11. D18 prevents the trigger pulse from appearing at the collector of Q15.

4.4.2.8 J-K Bistables

The J-K bistables M1a and M1b operate when the clock line goes negative:-

a) If J and K are of opposite level, i.e. J is high and K is low, or vice versa, these levels are transferred to the output.

b) If J and K are both high, the outputs will complement, i.e. Q high, $\overline{Q}$ low becomes Q low and $\overline{Q}$ high.

4.4.2.9 +5V Supply Stabiliser

An explanation of this circuit consisting of Q17, Q18, R59, R60, R61 and D21 is given in section 4.1.5 for the equivalent display board circuit.

4.4.2.10 FET Changeover Switch

In order that, when the 'continuous' mode is selected, the input to the Y deflection amplifier is isolated from the beam switch signal which is then fed to the X deflection amplifier, two FET changeover switches are used.

When SW2/4b is made, Q31 conducts. Thus, D29 conducts, causing Q30 to turn off and isolating the sweep input from R111. Also, with Q31 conducting, D30 is forward biased and, therefore, Q32 turns off, causing Q33 to conduct and feed the beam switch signal to R111.

With Q31 conducting, and therefore Q30 turned off, Q43 is turned off, thus isolating the Y deflection amplifier from the beam switch input. The Y deflection amplifier then takes up a steady state with both outputs at approximately A3 potential. When Q31 is turned off (because a mode other than 'continuous' has been selected), Q30 and Q43 turn on while Q33 turns off. This feeds the sweep input to the X deflection amplifier and the beam switch to the Y deflection amplifier.

4.4.2.11 Servo Amplifier (see also Camera Cassette Circuit C/11668/1)

4.4.2.11.1 Introduction

The function of the servo amplifier is to regulate motor speed and, thus, the paper speed. It must have a short response time to transient changes of load, adequate stability and accurate control of speed. Speed is variable between 0·5cm/s and 100cm/s (on standard units) by push-button speed controls on the front panel. Intermediate speeds can be obtained by pressing more than one button and adding their speeds.

4.4.2.11.2 Principle of Operation

The speed control signal is derived from the −12V rail through a resistor selected by the speed control buttons SW1. This is summed with a signal, proportional to motor speed, derived from the tachometer. The motor will run up to the speed at which the tachometer signal becomes effectively equal to the speed control signal, i.e., almost zero voltage at the amplifier summing junction. The output of the amplifier will then be at a level to hold the motor speed constant. Any variations in motor speed will modify the input signal to the amplifier and, hence, its output in such a sense as to restore the motor to its constant speed. The accuracy to which the speed may be held constant is determined by the tachometer characteristics, motor response and the gain/frequency response of the amplifier.

The block schematic diagram (Fig. 4.7) shows that there are three stages of amplification. The first amplifier (A) is situated in the camera cassette and acts as a non-inverting buffer stage between the tachometer and the main amplifier. The second amplifier (B) is situated on the camera control board and has preset controls to determine the maximum and minimum motor speeds. The third amplifier (C) is situated in the camera cassette and provides the current drive of the servo motor. Negative feedback is taken from the motor to the summing junction of the amplifier (B) and to its output drive stage.

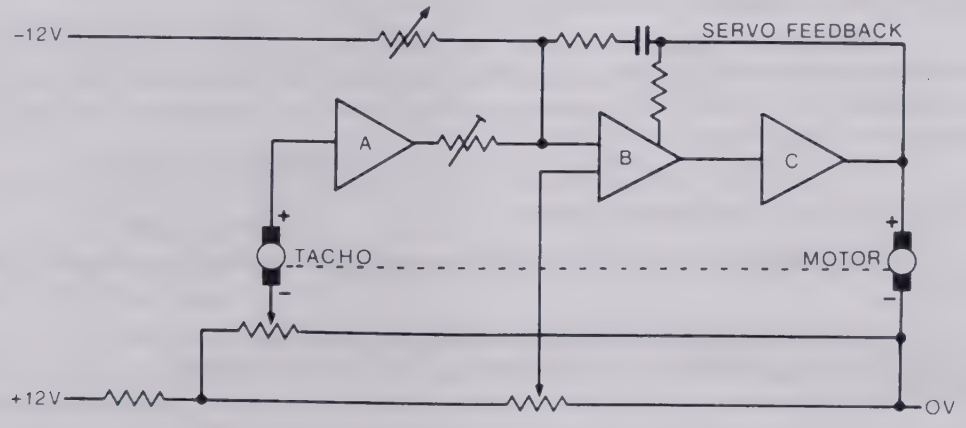


Fig. 4.7 Block Schematic Diagram - Servo Amplifier

4.4.2.11.3 Tachometer Buffer Amplifier Circuit

Q5 and Q7 form a non-inverting unity gain amplifier which minimises loading of the tachometer. Q5 is a dual transistor connected as an emitter coupled differential amplifier. Signal is taken from the positive output of the tachometer to the base of Q5a and the output from the collector of Q5a drives the base of Q7. Negative feedback is taken from the collector of Q7 to the base of Q5b to stabilise the gain and d.c. conditions of the amplifier. The output signal to the main servo amplifier is taken between the collector of Q7 and the negative output of the tachometer.

4.4.2.11.4 Servo Amplifier Circuit

The first stage of the amplifier comprises Q19 and Q20 connected as an emitter coupled differential amplifier. The non-inverting input is connected to RV12 which is adjusted to determine the minimum speed of the servo motor by balancing the amplifier. The negative side of the tachometer is returned to the junctions of R64, R65, which is at a potential of approximately 1·15V. This provides an initial signal level to the voltage follower. The positive side of the tachometer is connected to the inverting input of the differential amplifier through the input resistor comprising R68 and RV13. RV13 is adjusted to determine the maximum speed of the servo motor.

The base of Q19 is a summing junction which receives a fixed input from the speed selection switches and a feedback signal from the tachometer. The correct speed is obtained when the output current from the tachometer voltage follower becomes approximately equal to the current drawn by the speed selection network. The diode D25 ensures that the base of Q19 cannot go more than 0·6V positive of the base of Q20 when the negative speed selection current is switched off. The zener diode D26 provides coupling from the collector of Q19 to the base of Q21. This method of coupling permits a change of d.c. level without loss of signal amplitude. The collector current of Q21 provides drive to the output amplifier. Negative feedback from the servo motor is taken through R77 to the emitter of Q21 to stabilise d.c. conditions and a.c. feedback through C16 and R72 ensures fast response without overswing.

The servo motor may be switched on at a constant speed to provide a 'space' by switching on Q26. Alternatively, for continuous running in the RASTER mode or CONT mode, Q23 is switched on and draws its collector current through the speed control resistors selected by SW1.

4.4.2.11.5 Servo Motor Drive Amplifier

Q1 and Q2 are a complementary PNP/NPN pair which may be considered as a single transistor with very high current gain. When signal is received from Q21 in the main servo amplifier, Q1 provides base current to Q2 and holds Q3 cut off. The emitter current of Q2 drives the servo motor and negative feedback is taken from the emitter of Q2 to the main servo amplifier. When the signal from Q21 falls, i.e. the motor is to stop, Q1 and Q2 are switched off and the collector voltage of Q1 falls, enabling Q3 to conduct. Thus, the energy stored in the momentum of the armature is rapidly dissipated through Q3, giving regenerative braking and an almost instantaneous stop.

4.5 DFO6M Main Assembly (see Circuit Diagram C6/12445)

The DFO6 assembly contains the display and fibre-optic CRT's, the required printed circuit boards, power unit assembly and the front panel controls.

The power supplies are carried to the printed circuit boards in the main assembly via two plugs and sockets (SKT5 and SKT6) mounted on the power unit. The Display board and the Camera Control board are interconnected through the edge connectors SKT1 and SKT2 respectively; the beam switch connection is made by a low capacitance, coaxial cable.

Also mounted on the power unit is the socket SKT7, which provides all the necessary signal and logic connections to the amplifier module.

CRT connections are made directly from the boards supplying the deflection signal and plate voltages.

The colours of wiring insulation obey the following code:-

RED with WHITE trace (or WHITE with RED trace)	+240V
RED with GREEN trace	+28V
RED	+12V
RED (Heavy Insulation)	+4kV
BLACK	0V (Light Current)
BLACK with WHITE trace	0V (Heavy Current)
BLUE	-12V
VIOLET	-2kV
BROWN	CRT Heaters
GREEN	EARTH

4.5.1 Power Supplies (Circuit Diagram C/11707)

4.5.1.1 The power supplies are fitted to a sub-chassis at the rear of the DFO6 display unit. This enables the power pack to be tested before assembly with the main display unit (see 6.2.5 for power supply removal). The power pack supplies the following outputs:-

+12V regulated, stabilised and current limited to 1A
-12V regulated, stabilised and current limited to 1A
+28V at 4A, but fused at 3A
+240V at 120mA
-2000V, with overload limiting on the inverter input
+2000 or +4000V, with overload limiting on the inverter input.

All supplies are independently connected to a common 0V busbar which is grounded to chassis in the DFO6. A high current 0V line is brought out separately for the camera drive servo and stimulus output stages. A low current 0V line is used for all other circuitry in the main unit and module nesting unit. These precautions avoid interaction of supplies drawing heavy current or having large current fluctuations. Stabiliser board outputs are taken via short wiring to stand-off insulators which serve as distribution points for their outputs. The power supply module houses removable printed circuit boards for the +12V and -12V stabilisers, the -2000V, +2000V and +4000V E.H.T. supply and an audio amplifier to drive a 15Ω loudspeaker. Jack sockets are provided for the audio amplifier output and the footswitch input. A voltage selector is used with the split-primary mains transformer to accomodate a.c. mains inputs of 100 to 125V in 5V increments and 200 to 250V in 10V increments. The unit will work correctly with mains variations of +10% to -10% of nominal. A 12V indicator lamp is used to signify that the power supply is switched on. Green light from this illuminated push-button switch is transmitted via the transparent operating rod to the front panel.

4.5.1.2 Circuit Description

The 240V, 120mA supply is derived from a 200V secondary winding which is bridge rectified by MR1. C1 acts as a reservoir capacitor while R1 and C2 filter the d.c. output. It should be noted that C1 and C2 are housed in the same can. R3 is a current bleed to discharge the circuit when the unit is switched off. R1 is mounted between the audio and stabiliser printed circuit board sockets for easy access.

The 28V, 4A supply is obtained from a 22V secondary winding, bridge rectified by MR2 and with C3 acting as a reservoir capacitor. R2 provides a line trigger, referred to 0V.

The +12V, 1A and -12V, 0·5A supplies are bridge rectified by MR2 and MR4. C4 and C5 act as reservoirs and the output is fed to the stabiliser board.

R4 ties the 0V rail to earth in the event of the display socket being removed (for safety reasons).

4.5.2 Stabilised Power Supply (Circuit Diagram C/11460)

4.5.2.1 Principle of Operation

The +12V and -12V supplies are stabilised by circuits on a single plug-in card. The circuits are identical for both supplies.

An integrated circuit voltage regulator complete with internal reference performs the stabilising function. Extra current output capability is produced by using external pass transistors. Short circuit current limiting is incorporated.

4.5.2.2 Circuit Description

As the circuit diagram for the +12V and -12V supplies is identical, the circuit for the +12V stabiliser is described in detail.

The Monolithic Integrated Voltage Regulator (see Fig.4.8), M1, consists of a temperature compensated reference amplifier, error amplifier, a power output stage and a current limiting facility.

The voltage reference output is fed to the non-inverting input of the error amplifier, while the inverting input is used for sensing. The output, V OUT, drives Q1, the output current of M1 being limited by R2.

The emitter of Q1 supplies the base current of the series pass element Q2. The output voltage is fixed by the potential divider network R6 in series with R7, R8 in parallel. This potential is fed to the inverting input of the error amplifier as described previously.

R4 in parallel with R5 determines when the regulator current limit takes effect. When approximately 1A is being passed, 0·6V is produced across the Current Sense and Current Limit terminals which turns on a transistor in M1 and limits the drive available from V OUT.

Frequency compensation for M1 is accomplished by C1 connected from compensation to the inverting input of M1; C2 removes high frequency parasitic oscillations.

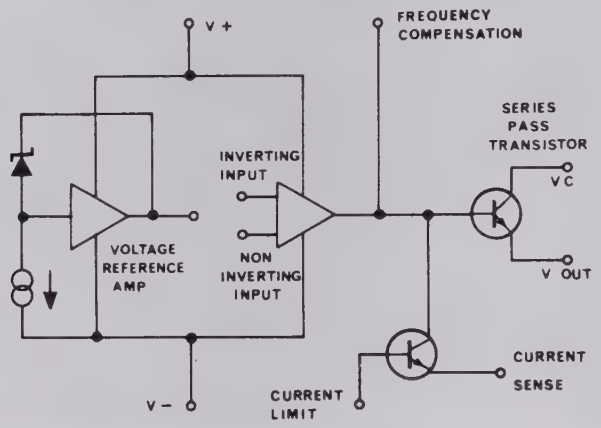


Fig. 4.8 Integrated Circuit Voltage Regulator - Block Diagram

4.5.3 Stabilised EHT Unit (Circuit Diagram C/11456)

4.5.3.1 Principle of Operation

To produce stable EHT voltages of +4kV, +2kV and −2kV from a d.c. to d.c. converter, the negative EHT output is sensed and used to regulate the d.c. input voltage. In the event of a short circuit on either or both outputs, the input current to the circuit is limited to 0·6A.

4.5.3.2 Circuit Description

If initially Q5 is turned on, as its base is receiving current through R4, Q6 is turned off. However, the supply voltage is dropped across the primary. Thus, the rate of change of flux produced induces an e.m.f. in the feedback winding. This ensures that the condition is maintained. When the core saturates, the induced voltage is reduced and the circuit regenerates. Square wave oscillation occurs at approximately 5kHz. The secondary produces a square wave voltage of 2kV peak-to-peak.

When the end of T1 secondary becomes positive, C2 charges and D2 conducts, but when the secondary becomes negative, C2 charges but this time D5 conducts and charges C6. D4 conducts on the next positive cycle as before, but when the secondary becomes negative for the second time, C2 will stay charged because D5 will no longer conduct as C6 is already charged. However, as the −2kV has always a load across it, C6 will gradually discharge until D5 conducts to replenish the charge into C6. R7 and C8 supply extra smoothing to the output, thus giving a ripple content of less than 0·02%.

The current to the primary of the transformer is regulated by Q2 which draws base current from the emitter of Q3. This current is controlled by the regulating amplifier Q4. When the −2kV line is correct, R8, R9 and R10 draw approximately 200μA and this is supplied from +12V through R5 and R6. RV1 is adjusted to set the −2kV rail at the correct level. Any variation in the −2kV line will then alter the base current of Q4, permitting a compensating current to flow through Q2 to the chopper.

The positive EHT voltage is produced in a similar fashion to the negative except that when the +2kV has been produced, a further stage of voltage doubling is added to produce +4kV. When a fault condition occurs, the current through R1 will increase until it is approximately 0·6A. This will produce a voltage of 0·7V across the base/emitter of Q1, switching it on. The collector current of Q1 is drawn from Q4, thus reducing the drive available to Q2. This protects the EHT circuits in fault conditions.

4.5.4 Audio Amplifier (see Circuit Diagram C/11458/1)

The audio amplifier is mounted on a plug-in board in the power supply. It has a voltage gain of 10 and is capable of delivering 2 Watts (r.m.s) into an internal or external loudspeaker of 15Ω. The output is protected against short or open circuit load. The audio bandwidth is from 50Hz to 15kHz (-3dB) with low distortion.

4.5.4.1 Circuit Description

The audio input comes from the gain control via C2. Resistors R1, R2 and R3 stabilise the input d.c. level. C1 prevents supply ripple from reaching the input. Q1 and Q2 operate in common emitter mode, with Q3 acting as an emitter follower for positive signals, and the combination of Q4 and Q5 acting as an emitter follower for negative signals. R6 drops sufficient voltage to eliminate crossover distortion. C4 reduces high frequency loop gain to prevent instability. R8 and R5 determine the gain of 5·6.

Low frequency cut-off is determined by C3 (L.S) = 3·75ms. This results in an overall low frequency cut-off of about 40Hz.

The circuit may be operated into a 3Ω loudspeaker with a low frequency cut-off of 200Hz, although power is slightly reduced. C5 reduces loop gain at high frequency to make the amplifier stable into any load. Transistors are rated for full power into any load, including short circuit.

4.6 The Amplifier Module

4.6.1 Introduction

4.6.1.1 The FOR-4.2 amplifier module is used with the display and fibre optic recorder DFO6M. The combination gives a display and recording unit with normal oscilloscope facilities. It is intended for measurement and recording of signals from d.c. to 120kHz. Signal input is via BNC sockets on the front panel. These are terminated to enable the use of standard probes and input leads. The module comprises a number of sub-assemblies, each of which will be described with respect to its circuit diagram.

4.6.1.2 The sub-assemblies with their circuit numbers are as follows:-

Y Amplifier	CD-043-14244-1
X Amplifier	CD-043-14243-1
Trigger Circuit	CD-043-14245-1

The interconnections between the sub-assemblies are shown on circuit diagram A1-043-14851.

4.6.2 The Y Amplifier

4.6.2.1 Input signal coupling is selected by SW1. When 'a.c.' is selected, a 150n capacitor is connected in series with the input signal. When 'gnd' is selected, the amplifier input is connected to 0V and the signal input socket is left open circuit. When 'd.c.' is selected, the input signal is connected directly to the input attenuator.

4.6.2.2 The sensitivity of the Y amplifier is selected by the input attenuator. This comprises two stages of capacitor compensated attenuation. The first stage divides the signal in decade steps and the second stage provides the intermediate 1.2.5 division. On the most sensitive range (10mV/div), the input signal is connected to the input of the amplifier without any attenuation. Variable capacitors are fitted in parallel with inputs to each of the attenuators enabling the input capacitance of the amplifier to be equalised for all sensitivities so that a probe may be used without re-adjustment on all ranges.

4.6.2.3 The signal from the attenuator is coupled to the input stage through the current limiting resistors R12 and R13. These protect the diodes D1 and D2 if an excessive voltage is applied to the input without adequate attenuation. C7 provides compensation for the capacitance of the diodes D1 and D2. The input stage comprises a dual FET connected as a source coupled pair. The constant current transistor Q2 provides a high source load to ensure optimum amplifier balance. Outputs are taken from both drains of the dual FET to provide a balanced input to the second amplifier stage. RV1 enables two outputs of Q1 to be accurately balanced; RV7 is used for phase shift equalisation.

4.6.2.4 The second stage uses the five transistors of M1 as a long tailed Darlington pair with a constant current transistor in the common emitter circuit. A single ended output is coupled through Q8 to the gain control RV2. Negative feedback is taken from the collector of Q8 to the gate of Q1b to set the gain of the first two stages to 10. R29 and C9 form a phase-advance circuit which protects against parasitic oscillation.

4.6.2.5 The next stage uses the five transistors of M2 in the same configuration as the previous stage. The nominal stage gain is 5 or 50 and may be adjusted by RV3 and RV4 respectively to calibrate the amplifier correctly. The preset potentiometers RV5 and RV6 adjust the d.c. level on the two gain ranges.

4.6.3 The X Amplifier

4.6.3.1 The X amplifier is very similar to the Y amplifiers in general and the same circuit description applies. The following differences should be noted:-

The 50V/div sensitivity range is not available as this switch position is used for internal sweep. There is no x 10 switch on the X amplifier and therefore the gain is calibrated by RV3 and d.c. output level is set by RV4. The third amplifier is used in the inverting mode and the negative feedback signal is therefore taken to the input base of M2.

4.6.4 The Trigger Circuit

4.6.4.1 The trigger circuit diagram shows all of the circuits mounted on the trigger printed circuit board. These include the Z modulation amplifier, the X-Y gate circuit and the trigger generation circuits.

4.6.4.2 The Z modulation signal amplifier employs Q13, Q14 and Q15 as a unity gain inverting amplifier. It has an input impedance of 100k and a very low output impedance. D20 protects the base/emitter junction of Q13 from excessive negative voltage excursions.

4.6.4.3 The transistors Q16 and Q17 are cut off when the X V/DIV is set to S and are switched on for all other positions of the V/DIV control. Thus, the collectors of Q16 and Q17 are held at +12V when the EXT X amplifier is in use and this inhibits the sweep generator by applying +12V to the T.B. CONTROL and + GATE lines.

4.6.4.4 The X-Y GATE signal is required to provide trace bright-up when recording X-Y plots. The gate signal may be supplied from an external source or may be generated from the record command when SW6 (internal preset) is set to MAN. When the RECORD switch or the FOOTSWITCH is operated, the junction of R80, R81 is connected to 0V through D21. Thus, Q18 is switched on and draws current through Q19. If SW6 is set to MAN, positive feedback through R85 will speed up the switch-on. A positive signal from Q18 collector or from the EXT GATE socket on the rear of the module will cause Q20 to conduct, cutting off Q21 and so enabling the X-Y GATE line to go high.

4.6.4.5 The trigger signal may be derived from either the EXT TRIGGER input or from any one or more of the Y signal channels. SW2 selects a.c. or d.c. coupled by short circuiting C1 (EXT) or C2. Note that, in the AUTO trigger mode, the signal is always a.c. coupled as the AUTO/NORMAL switch SW5 is connected in series with SW2. The four poles of SW1 select the Y channel or channels from which an internal trigger signal may be generated. The input resistors are arranged to reduce the gain per channel as more channels are switched to provide mixed triggering.

4.6.4.6 The EXT TRIG signal is fed to the buffer amplifier through R22. The diodes D1 and D2 protect Q1 against excessive input signals and the resistor R22 limits the current in the diodes. Q1 is connected as an emitter follower to provide a high impedance. The output of Q1 is taken from the junctio of R25, R26 and this point is set to 0V by RV2. The EXT TRIG signal from Q1 or the internal trigger signal from SW1 is selected by SW3 and fed to the base of Q2. Negative feedback is taken from the collector of Q2 through R20 to the base of Q2 to set the gain of the stage. RV1 is adjusted to set the d.c. conditions in the trigger amplifiers to ensure stable triggering from small signals. The output from Q2 is connected to the trigger differential amplifier and to the peak detector.

4.6.4.7 The peak detector is used in the AUTO trigger mode to develop the potential applied to the level control. The signal is a.c. coupled to the inverting input of M1a and the non-inverting input of M1b. As the signal at the input of M1a moves positive, the collector of Q3 will also move positive, charging C6 through R33. Similarly, a negative signal at the input of M1b will cause the output of M1b to move negative, charging C5 through R31. The potentials stored in C5 and C6 are applied to the LEVEL control, enabling the trigger point on the waveform to be accurately selected over the full peak-to-peak amplitude of the signal. When NORMAL triggering is selected, the peak detector circuit is not used and the LEVEL control is connected between +12V and -12V through R34 and R36 respectively.

4.6.4.8 The trigger differential amplifier comprises the emitter coupled transistors Q5 and Q7 with the constant current transistor Q6 providing the high impedance emitter load. Slope polarity of the triggering signal is selected by SW4. When positive slope is selected, the collector of Q5 is connected to +12V

through D8 and the signal is taken from the collector of Q7. When negative slope is selected, the signal is taken from the collector of Q5 and the collector of Q7 is held at +12V through D11. Q8 is a level shifting buffer amplifier which is controlled by the LEVEL control and provides the d.c. level to the base of Q7. Thus, adjustment of the LEVEL control changes the threshold of the differential amplifier to select the part of the signal which is amplified and used to generate the trigger pulse.

4.6.4.9 The output from the differential amplifier is buffered by the emitter follower Q9 and is then fed to the Schmitt trigger circuit which generates fast moving positive and negative edges from the incoming signal. The positive edge, coupled through C7, switches off Q4, enabling the timebase circuit. During the sweep, the + GATE signal is at +12V and this is connected through D15 to prevent transmission of further positive edges. The negative edge has no effect.

4.6.4.10 When the AUTO trigger mode is selected, the emitter potential of Q4 is supplied by the input verification monostable comprising M1c, M1d and Q12. Positive signals at the collector of Q11 are inverted by M1c to produce a negative output which charges C11. Thus, a smoothed negative level is applied to the input of M1d. This amplifier is connected as a comparator with hysteresis; its output will be positive when a trigger signal is available at the input of M1c. This positive level switches on Q12, enabling current to flow through D17. This causes the emitter potential of Q12 to rise to +12V, holding the timebase through Q4. The sweep is then triggered by cutting off Q4 as before. If there is no signal available in the AUTO mode, C11 discharges to 0V; the output of M1d falls; Q12 is cut off and the collector potential of Q4 falls to +5V. This enables the timebase to free-run.

A1.4 NEGATIVE LOGIC NOR GATE

Symbol:-

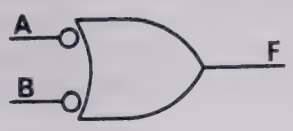


Fig. A1.3

The truth table for this gate is the same as for the NAND gate in terms of voltage levels, but as negative logic is used, it can be seen that the NOR function is satisfied if either A or B is LOW (1) and output F is HIGH (0) See Table A1.3.

A	B	F
HIGH (0)	LOW (1)	HIGH (0)
LOW (1)	HIGH (0)	HIGH (0)
LOW (1)	LOW (1)	HIGH (0)
HIGH (0)	HIGH (0)	LOW (1)

Table A1.3

A1.5 SUMMARY

It can be seen from the preceding that the logical function required is obtained when the gate inputs have logical 1 states in either the positive or negative logic cases.

The full list of logical functions is shown in Fig. A1.4 (obtained from MIL-STD-806B 26th Feb.1962 - Page 6).

A1.6 J.K. FLIP FLOP

This device is a development of the Reset/Set Bistable

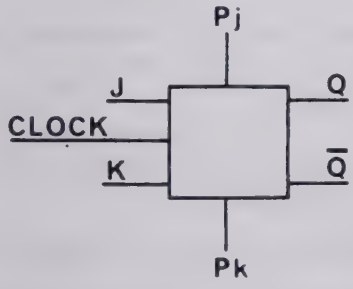


Fig. A1.5

Its principal advantage is that the input states can be transferred to the output by means of a clock input.

J.K. FLIP-FLOP TRUTH TABLE POSITIVE LOGIC

tn		tn + 1	
J	K	Qn	$\overline{Q}$n
LOW (0)	LOW (0)	Qn	$\overline{Q}$n
LOW (0)	HIGH (1)	LOW (0)	HIGH (1)
HIGH (1)	LOW (0)	HIGH (1)	LOW (0)
HIGH (1)	HIGH (1)	$\overline{Q}$n	Qn

Table A1.4

APPENDIX A1 BASIC LOGIC

A1.1 LOGIC INTRODUCTION

There are two types of logic, positive and negative logic. In the positive case, a typical logical 1 and logical 0 are high and low voltages respectively, whereas the converse is true for negative logic.

To simplify the explanation of the logic functions, HIGH and LOW will be used for voltage levels. There are a number of different logical functions used; those which are used in this equipment are detailed below:-

A1.2 POSITIVE LOGIC NAND GATE

Symbol:-

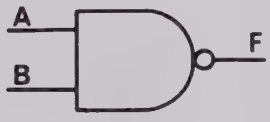


Fig. A1.1

The explanation of the gate is best shown by drawing a truth table, Table A1.1

A	B	F
HIGH (1)	HIGH (1)	LOW (0)
LOW (0)	HIGH (1)	HIGH (1)
HIGH (1)	LOW (0)	HIGH (1)
LOW (0)	LOW (0)	HIGH (1)

Table A1.1

e.g., when inputs A and B are HIGH, F is LOW, giving the function NAND.

A1.3 POSITIVE LOGIC NOR GATE

Symbol:-

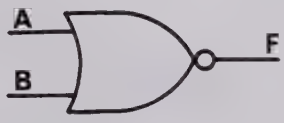


Fig. A1.2

The truth table for this gate is shown in Table A1.2.

A	B	F
HIGH (1)	HIGH (1)	LOW (0)
HIGH (1)	LOW (0)	LOW (0)
LOW (1)	HIGH (1)	LOW (0)
LOW (0)	LOW (0)	HIGH (1)

Table A1.3

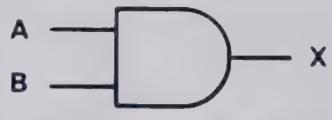
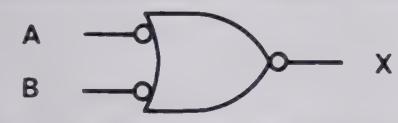
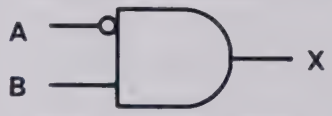
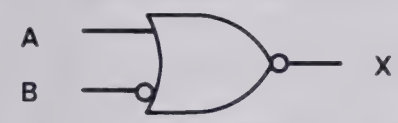
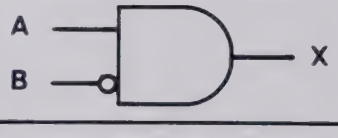
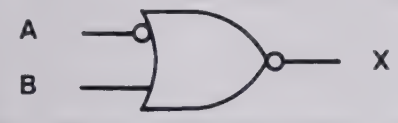
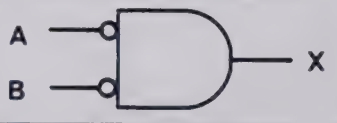
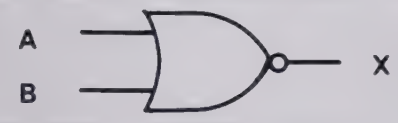
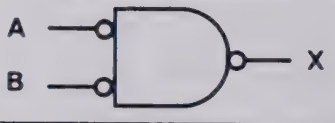
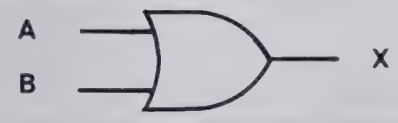
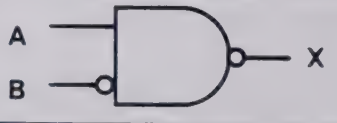
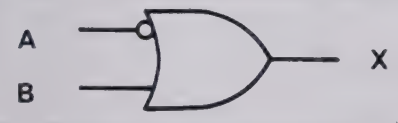
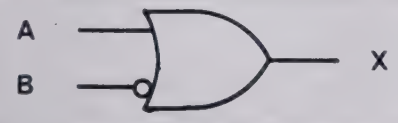
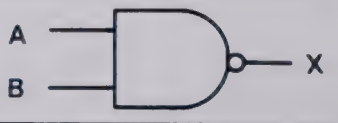
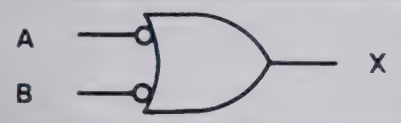
Hence the output is LOW when A or B (or both) are HIGH, giving the function NOR.

For the foregoing truth table, the conditions at time tn are the inputs before the clock pulse has arrived. The output conditions at time t(n+1) are those after the clock pulse has arrived. When J and K inputs are at the same level, the outputs will either (a) not change or (b) complement as shown. However, if the inputs are at opposite levels, the outputs will always go to the states shown for the two cases.

A voltage going from high to low on input Pj (sometimes referred to as CLEAR) will cause output Q to become LOW (0). Similarly, the same condition of Pk (sometimes referred to as PRESET) will cause output $\overline{Q}$ to become LOW (0).

When inputs are applied to either Pj or Pk (NOT simultaneously) the outputs go to the state described irrespective of the condition on J, K, or the clock input.

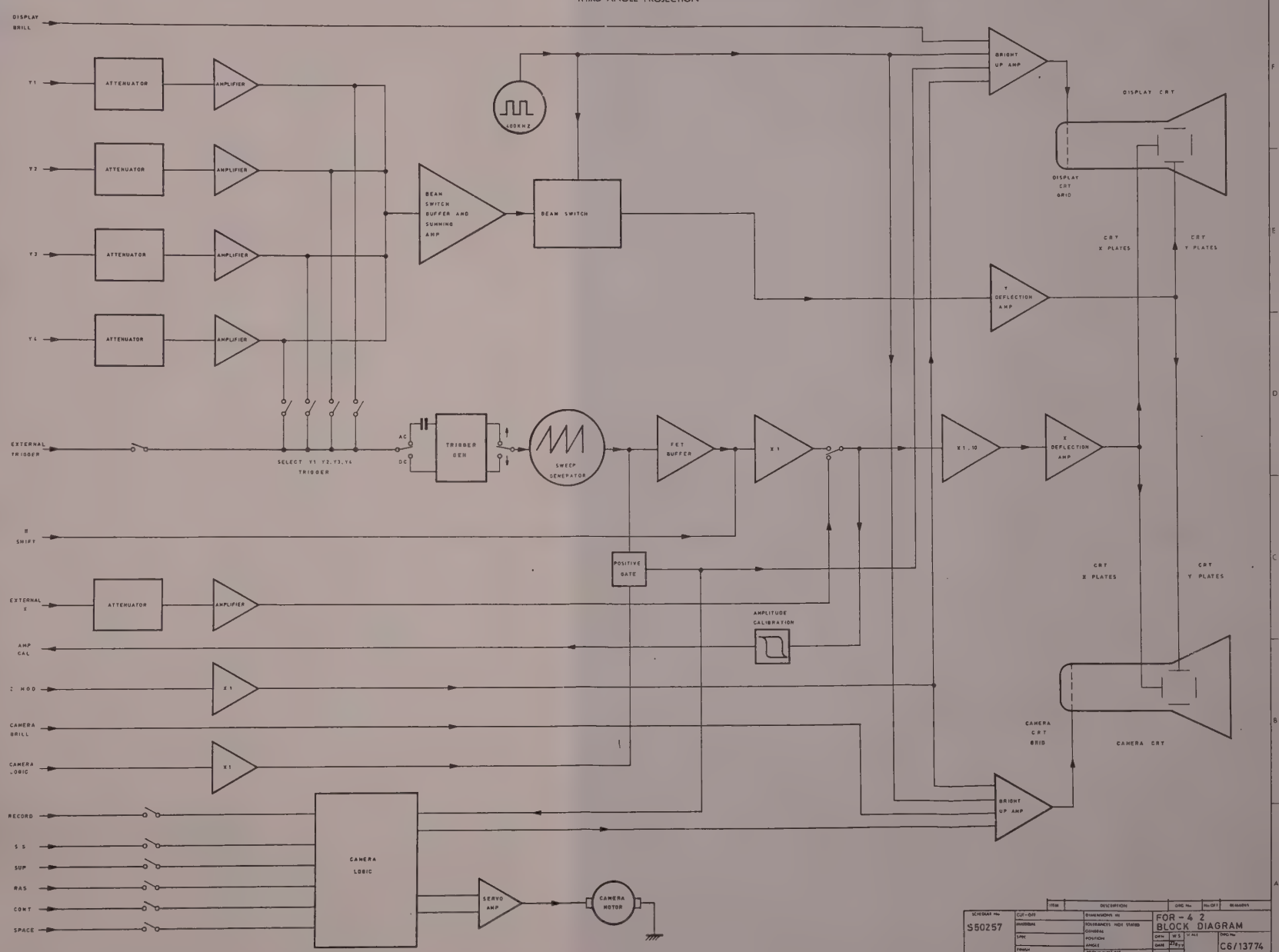
TABLE OF COMBINATIONS

AND	OR	A	B	X
		H H L L	H L H L	H L L L
		H H L L	H L H L	L L H L
		H H L L	H L H L	L H L L
		H H L L	H L H L	L L L H
		H H L L	H L H L	H H H L
		H H L L	H L H L	H L H H
		H H L L	H L H L	H H L H
		H H L L	H L H L	L H H H

C6/13774

ISSUE	MODIFIC ATIONS
C	20 10 76
1	3 2 77

THIRD ANGLE PROJECTION



SCHEDULE No	CUT-OUT	DIMENSIONS ARE	TOLERANCES UNLESS STATED	GENERAL	POSITION	ANGLE	TOOL/GAUGE REF
S50257							

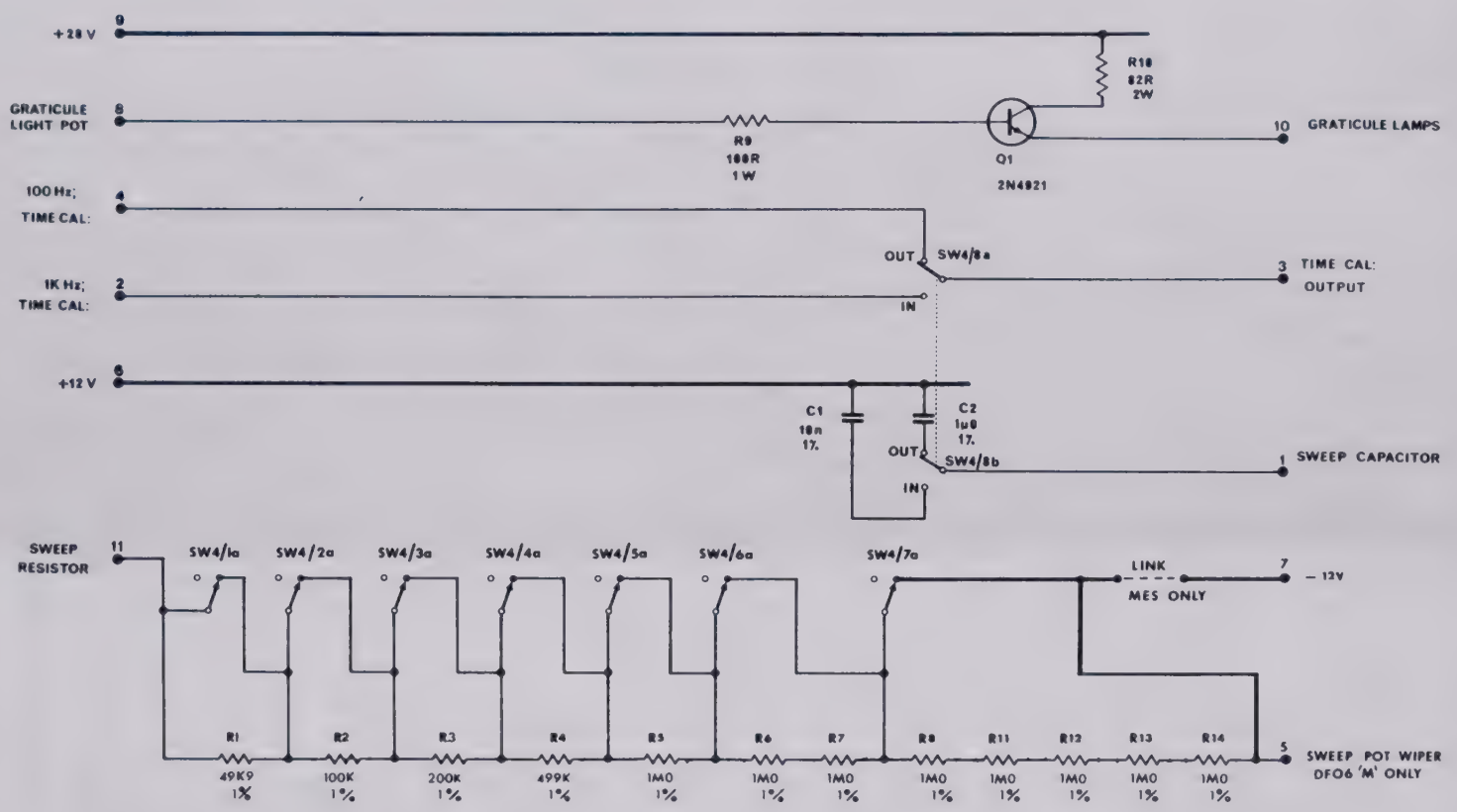
FOR-4 2
BLOCK DIAGRAM

DRN	WS	SCALE	DWG No
DATE	27/8/77		C6/13774
CHK			

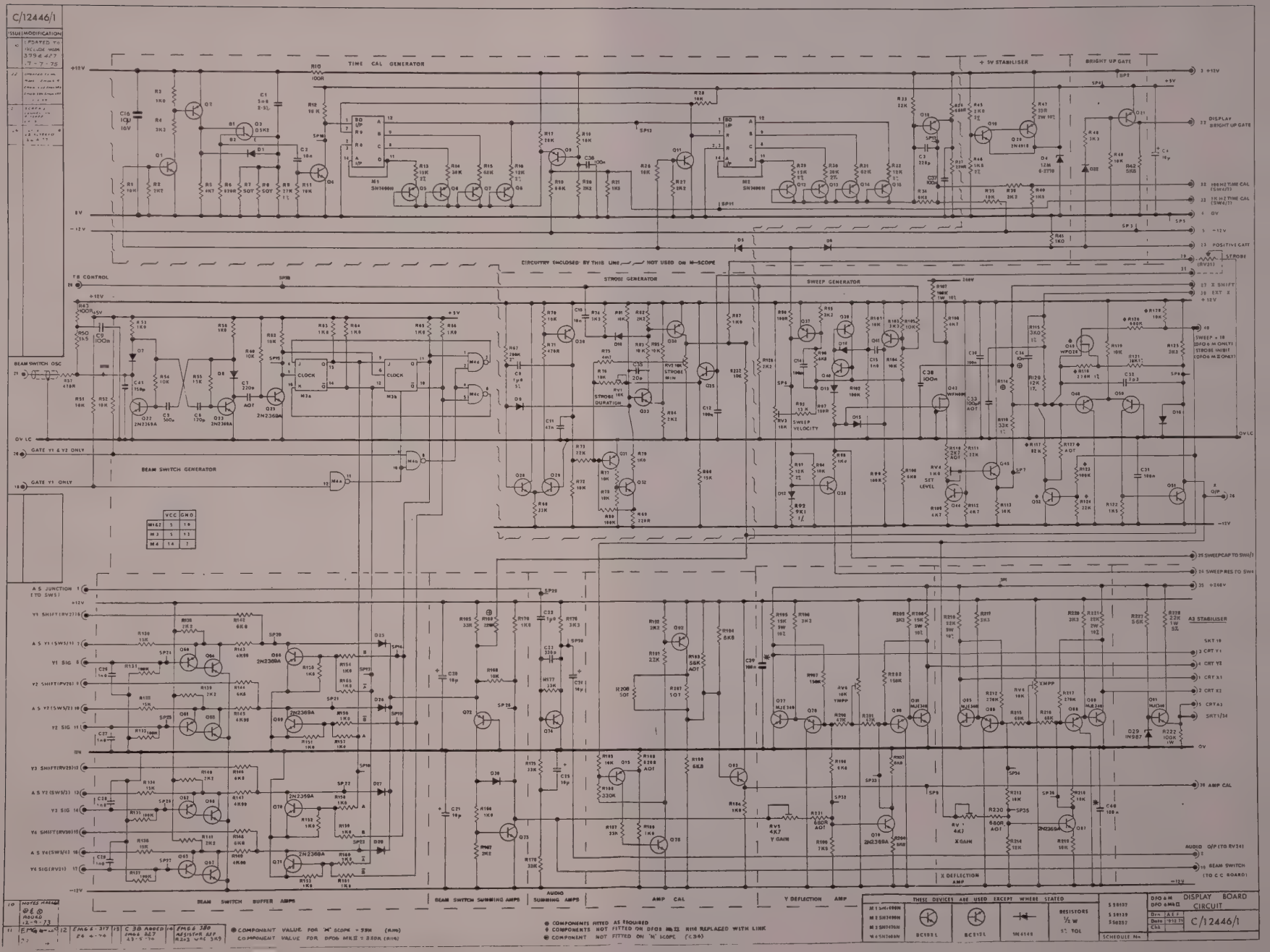
MEDELEC LTD

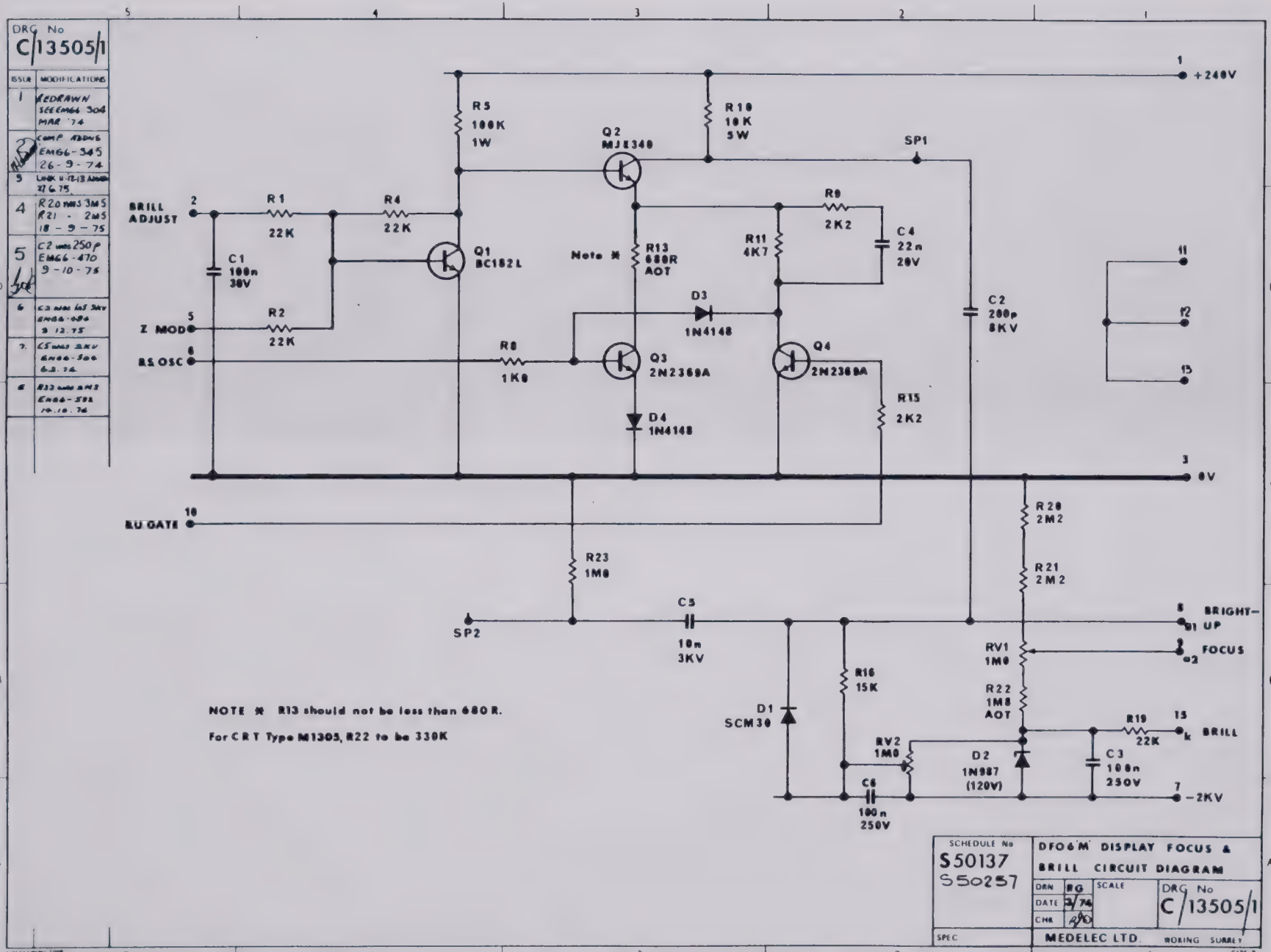
DRG. No
C/12448/1

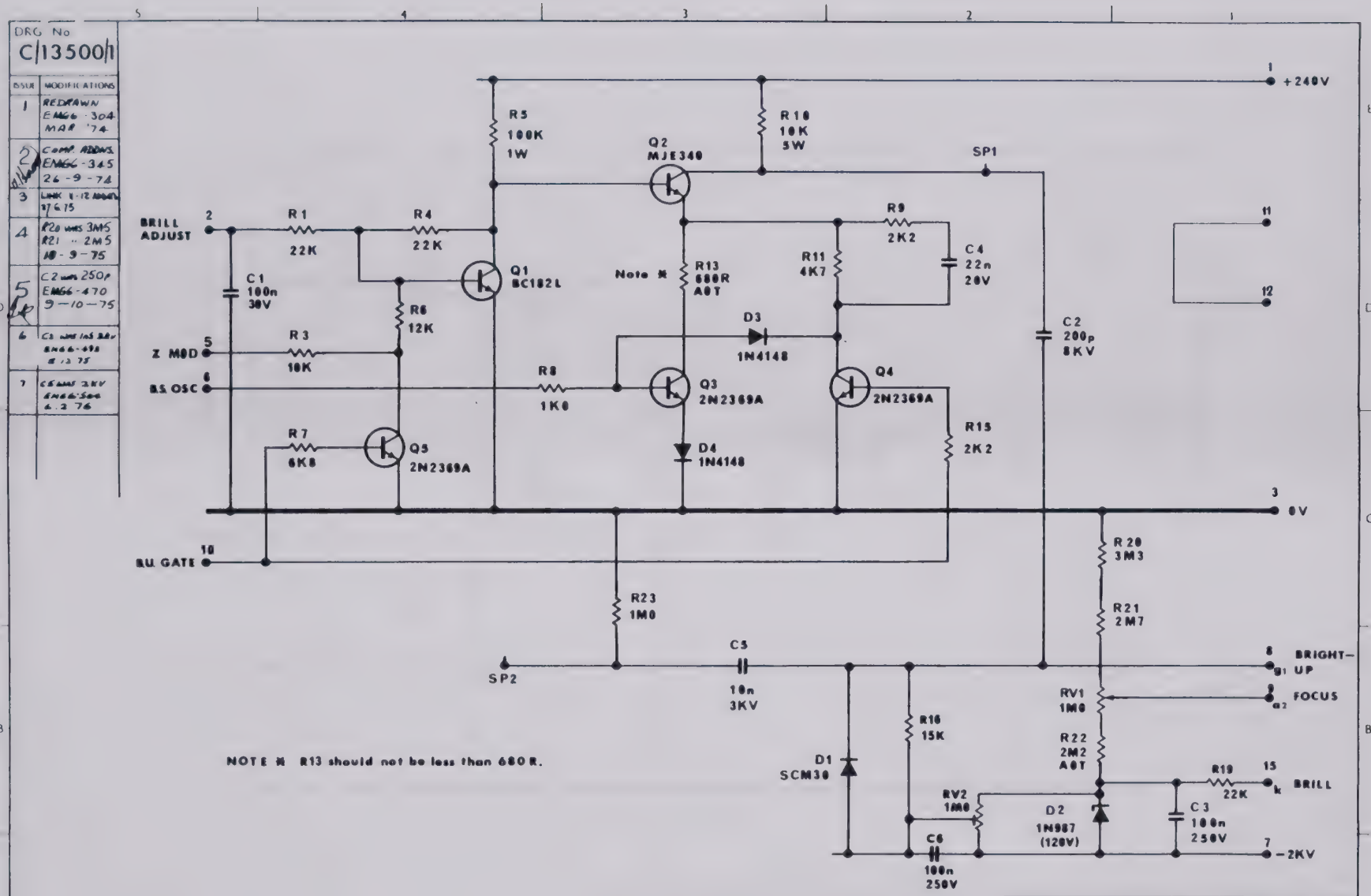
ISSUE	MODIFICATIONS
1	26-4-71
2	SW4/1 TO SW4/7 b SECTIONS SW4/8 C & D SECTIONS DELETED — BRILL. CONTROL 1&2 DELETED — TERMINATION POINTS RE-No4. R6 R7 & R8 WERE 5%. R2 R3 & R5 WERE 2%. C1 & C 2 WERE 2 1/2%. M-SCOPE SWEEP MOD. ADDED 1-12-71
3	EMG-6-888 1-3-72
4	PIN 4 100Hz WAS 1KHz PIN 2 1KHz WAS 100Hz Mod EMG 6/252 2-1-74
5	RESISTORS Added and value changed EMG6-355. 2-9-74.



SCHEDULE No. S.50137 S.50138	DFO6 MkII / DFO6 'M' } SWEEP VELOCITY P.C.B. CIRCUIT DIAGRAM		
	DRN. E.A.H.	SCALE —	DRG. No. C/12448/1
	DATE 26/4/71		
	CHK.		
SPEC.	MEDELEC LTD. WOKING, SURREY.		SIZE 2.


C/12446/1
ISSUE MODIFICATION
TIME CAL GENERATOR
+5V STABILISER
BRIGHT UP GATE
CIRCUITRY ENCLOSED BY THIS LINE NOT USED ON M-SCOPE
T/B CONTROL
STROBE GENERATOR
SWEEP GENERATOR
BEAM SWITCH OSC
BEAM SWITCH GENERATOR
A3 STABILISER
X DEFLECTION AMP
BEAM SWITCH BUFFER AMPS
BEAM SWITCH SUMMING AMPS
AUDIO SUMMING AMPS
AMP CAL
Y DEFLECTION AMP
DISPLAY BOARD CIRCUIT
C/12446/1


DRG No C/13505/1
ISSUE MODIFICATIONS
1 REDRAWN SEE EM66 308 MAR '74
2 COMP ADDED EM66-345 26-9-74
3 LINK U-12-13 ADDED 21.6.75
4 R20 was 3M3 R21 - 2M3 18-9-75
5 C2 was 250p EM66-470 9-10-75
6 C3 was 6n8 3kV EM66-484 9.12.75
7 C5 was 3KV EM66-506 6.2.76
8 R33 was 4M3 EM66-592 19.10.76
+240V
SP1
R5 100K 1W
R10 10K 5W
Q2 MJE340
BRILL ADJUST
R1 22K
R4 22K
C1 100n 30V
Q1 BC182L
Note ※
R13 680R AOT
R11 4K7
R9 2K2
C4 22n 20V
D3 1N4148
C2 200p 8KV
Z MOD
R2 22K
R8 1K8
Q3 2N2369A
Q4 2N2369A
R15 2K2
D4 1N4148
0V
BLU GATE
R20 2M2
R21 2M2
R23 1M8
SP2
C5 10n 3KV
BRIGHT-UP
FOCUS
RV1 1M8
R16 15K
R22 1M8 AOT
D1 SCM30
R19 22K
BRILL
RV2 1M8
D2 1N987 (120V)
C3 100n 250V
C6 100n 250V
-2KV
NOTE ※ R13 should not be less than 680 R.
For C R T Type M1305, R22 to be 330K
SCHEDULE No S50137 S50257
DF06M DISPLAY FOCUS & BRILL CIRCUIT DIAGRAM
DRN BG SCALE
DATE 3/74
CHK
DRG No C/13505/1
SPEC
MEDELEC LTD. WOKING SURREY
SIZE 2


DRG No C/13500/1
ISSUE MODIFICATIONS
1 REDRAWN EMG6-304 MAR '74
2 COMP. ADDED EMG6-345 26-9-74
3 LINK 8-12 ADDED 17.6.75
4 R20 WAS 3M3 R21 = 2M5 10-9-75
5 C2 was 250p EMG6-470 9-10-75
6 C3 was 1n5 3KV EMG6-498 11.12.75
7 C5 was 2KV EMG6-506 6.2.76
+240V
0V
BRILL ADJUST
Z MOD
B.S. OSC
BLU. GATE
SP1
SP2
R1 22K
R3 10K
R4 22K
R5 100K 1W
R6 12K
R7 6K8
R8 1K0
R9 2K2
R10 10K 5W
R11 4K7
R13 680R A0T
R15 2K2
R16 15K
R20 3M3
R21 2M7
R22 2M2 A0T
R23 1M0
RV1 1M0
RV2 1M0
R19 22K
C1 100n 30V
C2 200p 8KV
C3 100n 250V
C4 22n 20V
C5 10n 3KV
C6 100n 250V
Q1 BC182L
Q2 MJE340
Q3 2N2369A
Q4 2N2369A
Q5 2N2369A
D1 SCM30
D2 1N987 (120V)
D3 1N4148
D4 1N4148
Note X
BRIGHT-UP
FOCUS
BRILL
-2KV
NOTE X R13 should not be less than 680R.
SCHEDULE No
S50137
S50101
S.50257
DFO6M CAMERA FOCUS & BRILL CIRCUIT DIAGRAM
DRN BG
DATE 3/74
CHK
SCALE
DRG. No C/13500/1
SPEC
MEDELEC LTD WOKING SURREY
SIZE 2

DRG No C/11668/1	
ISSUE	MODIFICATIONS
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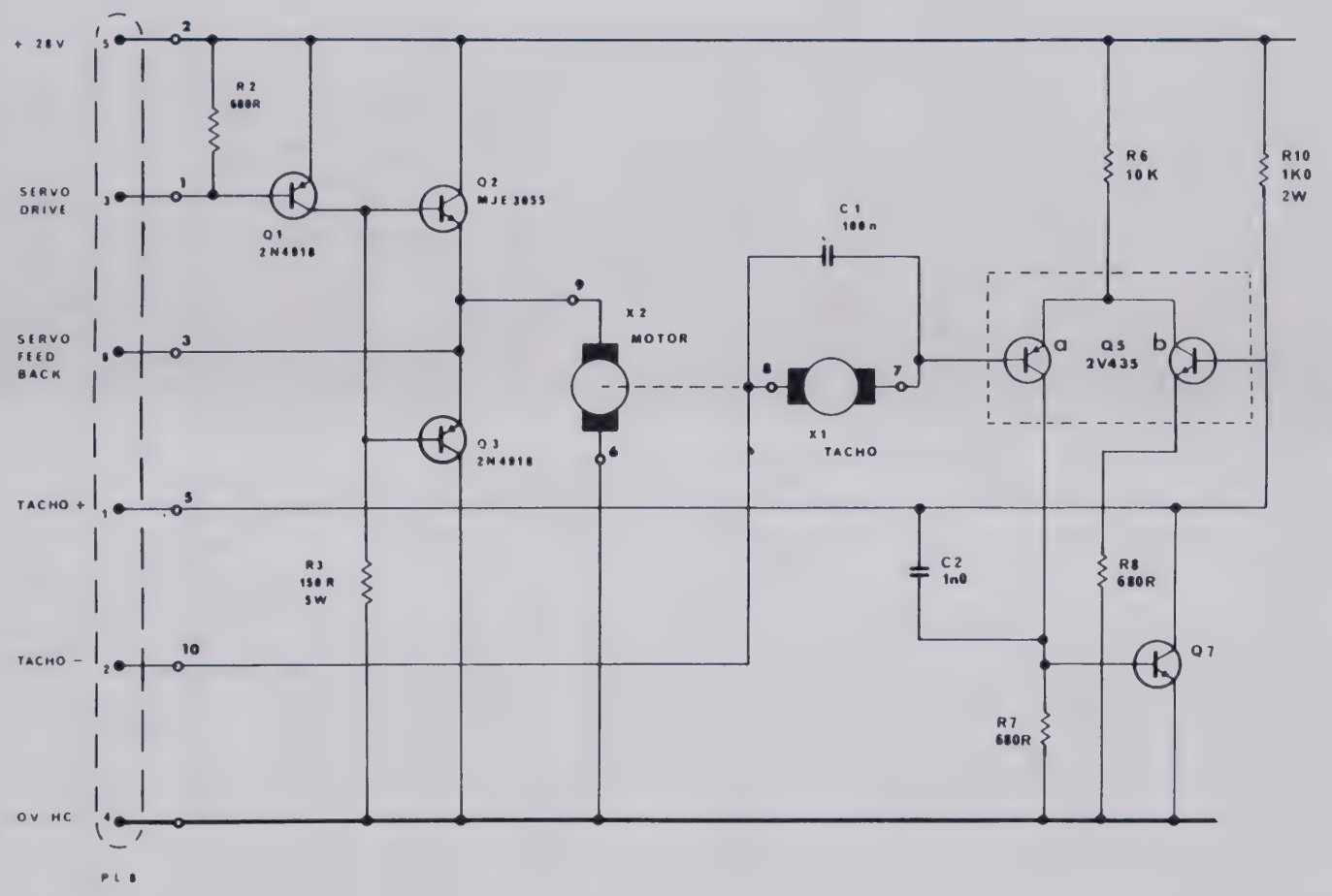
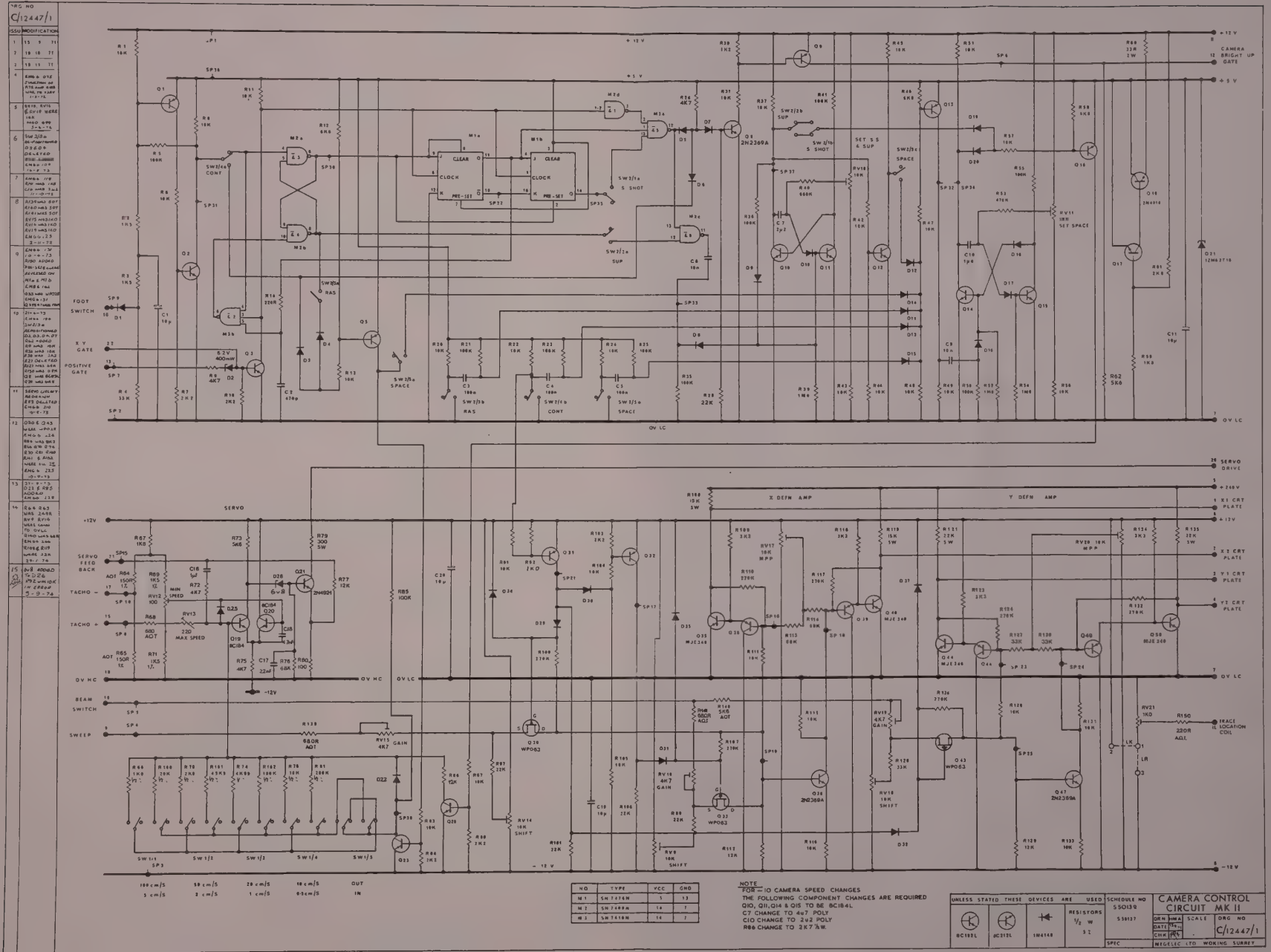
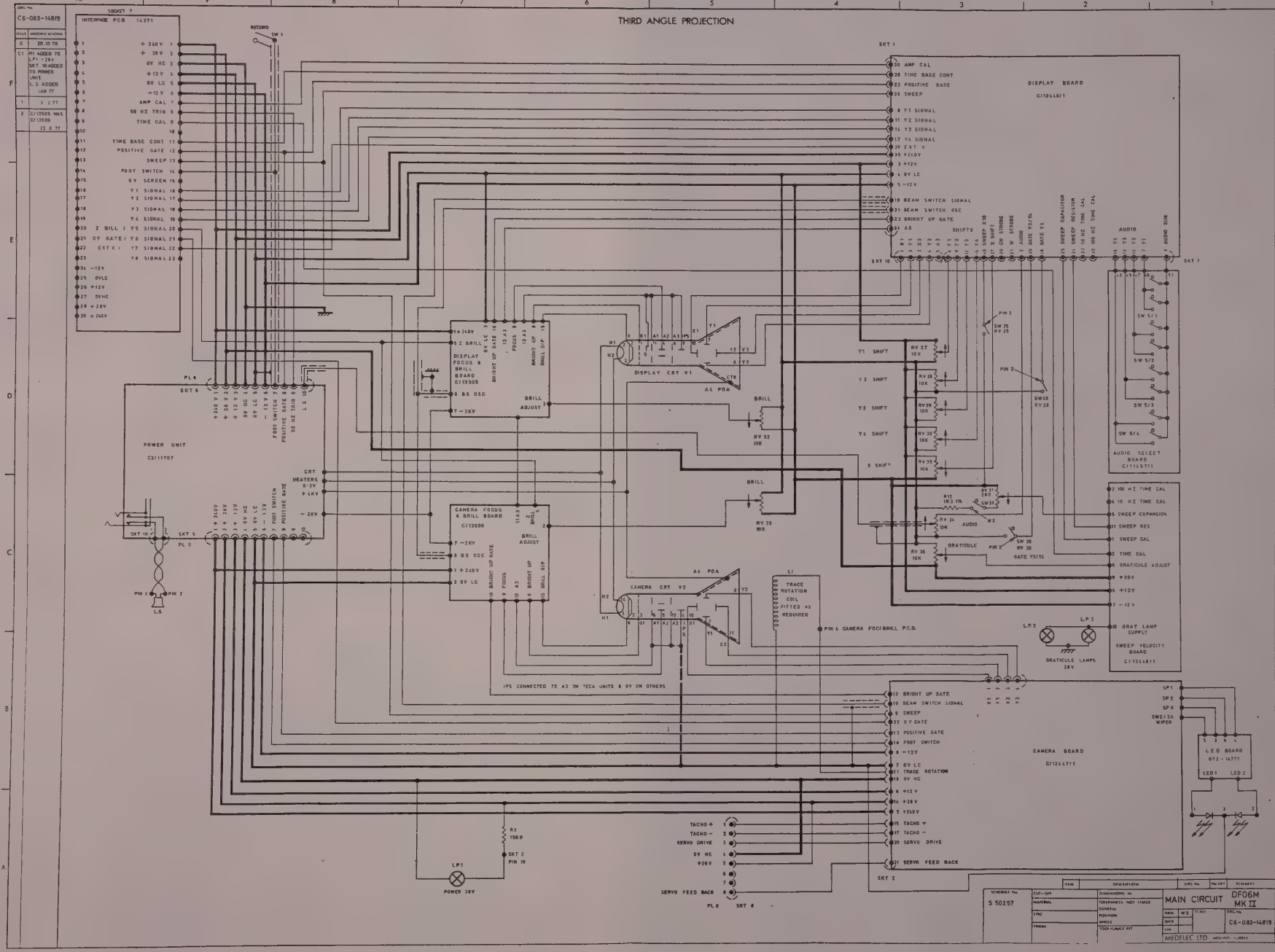
4	UPDATED TO INCLUDE EM66 206 21-3-74



THESE DEVICES ARE USED EXCEPT WHERE STATED			RESISTORS 1/2 W 5% TOL	SCHEDULE No S 58082	CAMERA CASSETTE CIRCUIT	
BC 182L	BC 212L			SPEC	DRN HMA SCALE	DRG No C/11668/1
					DATE 4 3 70	
					CHK	
					MEDELEC LTD WORING, SURREY	SIZE A


DRG NO C/12447/1
ISSU MODIFICATION
+12V
+5V
-12V
0V LC
0V HC
FOOT SWITCH
X Y GATE
POSITIVE GATE
CAMERA BRIGHT UP GATE
SERVO DRIVE
SERVO FEED BACK
TACHO -
TACHO +
BEAM SWITCH
SWEEP
X DEFN AMP
Y DEFN AMP
X1 CRT PLATE
X2 CRT PLATE
Y1 CRT PLATE
Y2 CRT PLATE
TRACE LOCATION COIL
SET S S & SUP
S SHOT
SUP
SPACE
RAS
CONT
100 cm/s
50 cm/s
20 cm/s
10 cm/s
0·5cm/s
5 cm/s
2 cm/s
1 cm/s
OUT
IN
NOTE
FOR — 10 CAMERA SPEED CHANGES
THE FOLLOWING COMPONENT CHANGES ARE REQUIRED
Q10, Q11, Q14 & Q15 TO BE BC184L
C7 CHANGE TO 4u7 POLY
C10 CHANGE TO 2u2 POLY
R86 CHANGE TO 2K7 ¼W.
UNLESS STATED THESE DEVICES ARE USED
BC182L
BC212L
1N4148
RESISTORS ½ W 5%
SCHEDULE NO 550139
538137
CAMERA CONTROL CIRCUIT MK II
DRN SHEA
DATE 15-1-
CHK RK
SCALE
DRG NO C/12447/1
SPEC
NEGELEC LTD WOKING SURREY


THIRD ANGLE PROJECTION
C6-083-14819
SOCKET 7
INTERFACE PCB 14371
RECORD
SW 1
SKT 1
DISPLAY BOARD
C/12648/1
SKT 10
SKT 1
SHIFTS
AUDIO
AUDIO SELECT BOARD
C/11457/1
POWER UNIT
C3/11707
PL 6
SKT 8
PL 5
SKT 5
SKT 10
LS
PIN 1
PIN 2
CRT HEATERS 6·3V
+4KV
-2KV
DISPLAY FOCUS & BRILL BOARD C/13505
CAMERA FOCUS & BRILL BOARD C/13600
BRILL ADJUST
DISPLAY CRT Y1
A4 PCB
CAMERA CRT Y2
TRACE ROTATION COIL FITTED AS REQUIRED
PIN 4 CAMERA FOCI BRILL P.C.B.
IPS CONNECTED TO A3 ON TECA UNITS & 0V ON OTHERS
Y1 SHIFT
Y2 SHIFT
Y3 SHIFT
Y4 SHIFT
X SHIFT
BRILL
GRATICULE
AUDIO
RV 27 10K
RV 28 10K
RV 29 10K
RV 30 10K
RV 35 10K
RV 32 10K
RV 28 10K
RV 34 10K
SW 40 RV 28
SW 30 RV 30
SW 31 RV 31
SW 5/1
SW 5/2
SW 5/3
SW 5/4
LP 2
LP 3
GRATICULE LAMPS 28V
SWEEP VELOCITY BOARD C/12648/1
CAMERA BOARD C/12647/1
LED BOARD 072-14771
LED 1
LED 2
SW 2/1 WIPER
SW 2/2A WIPER
R1 150R
LP1
POWER 28V
TACHO +
TACHO −
SERVO DRIVE
0V HC
+28V
SERVO FEED BACK
PL 8
SKT 6
SKT 2
PIN 19
MAIN CIRCUIT
DF06M MK II
MEDELEC LTD

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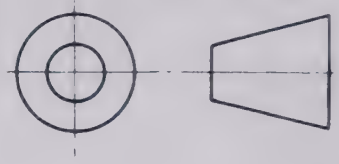
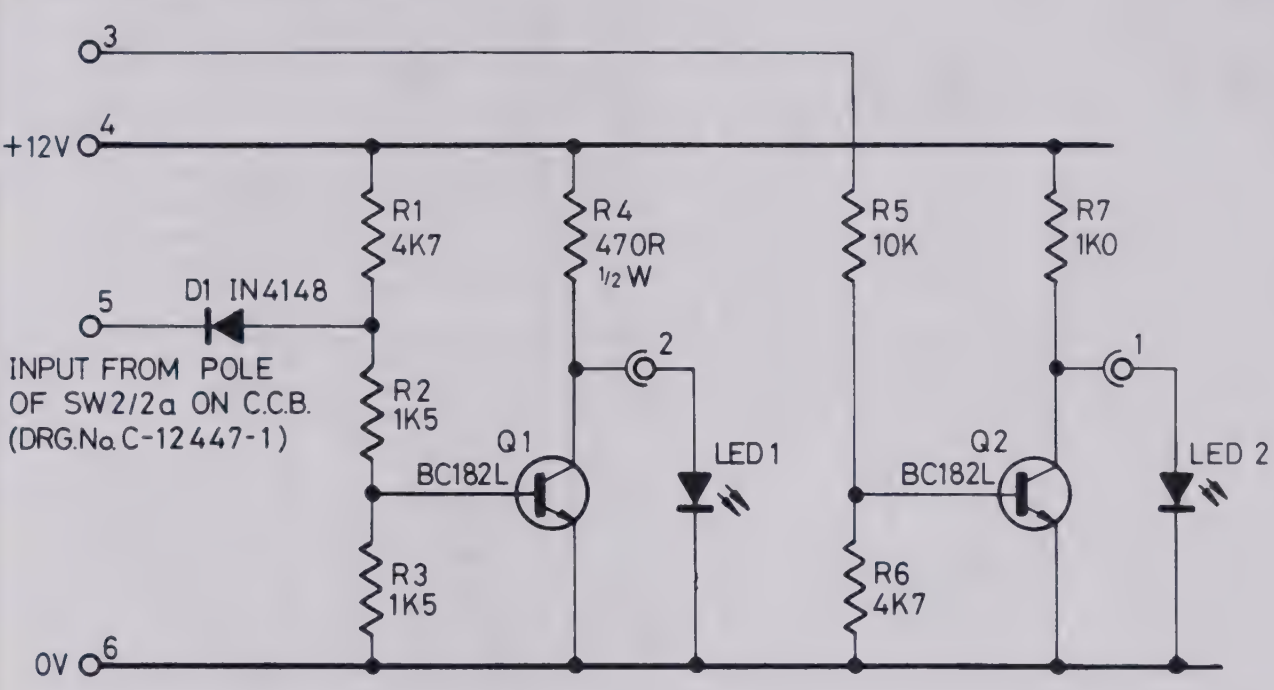
THIRD ANGLE PROJECTION



IF IN DOUBT - ASK

INPUT FROM PIN 12 OF C.C.B (DRG.No.C-12447-1) EDGE CONNECTOR (B.U. GATE)



LED 1
"READY"
(GREEN)

LED 2
"RECORDING"
(YELLOW)

NOTE

1 ALL RESISTORS TO BE 1/4W 5% UNLESS OTHERWISE STATED.

DIMENSIONS APPLY AFTER FINISHING AND ARE IN

DO NOT SCALE

	4.2.77	4.8.76	DATE	S50190 & S50257
			CHANGE	
	1	C	ISSUE	SCHD No.

TITLE
FOR-4 MkII & FOR-7 INDICATOR BOARD MkII
CIRCUIT DIAGRAM.

DRAWN CC-B.	DATE 4.8.76	TOLERANCES EXCEPT WHERE OTHERWISE STATED
TRACED	DATE	1 Place Decimal ± / 2 Place Decimal ± / 3 Place Decimal ±
CHECKED G.H.R.	DATE 4-8-76	SURFACE FINISH √
APPROVED	DATE	Angular Dimensions ±
		Hole Diameters + −
		Remove all burrs and sharp edges

SCALE

FIRST USED ON

TOOL/GAUGE REF

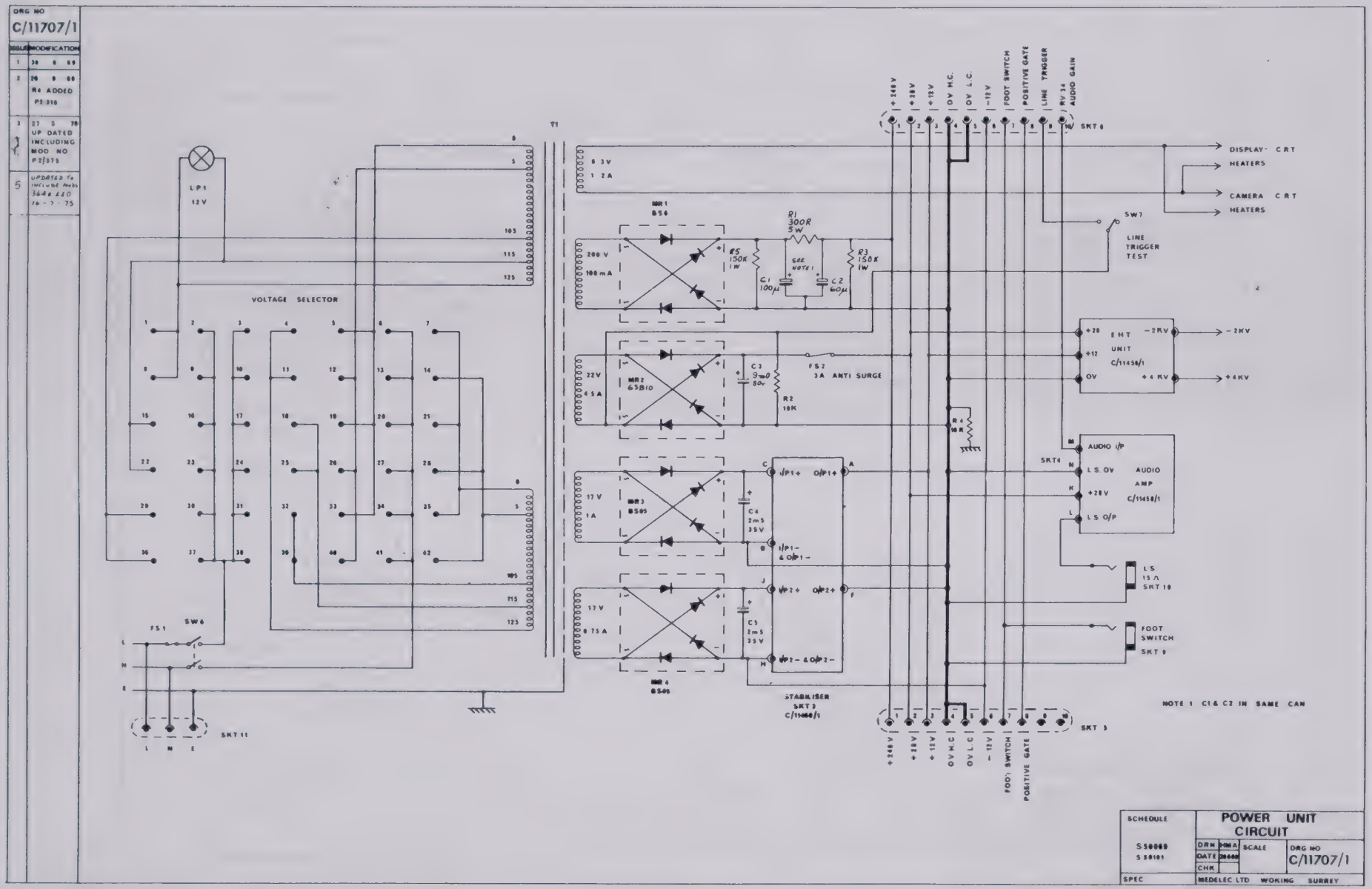
MATERIAL

FINISH

MEDELEC LTD.,
WOKING, SURREY. ENGLAND

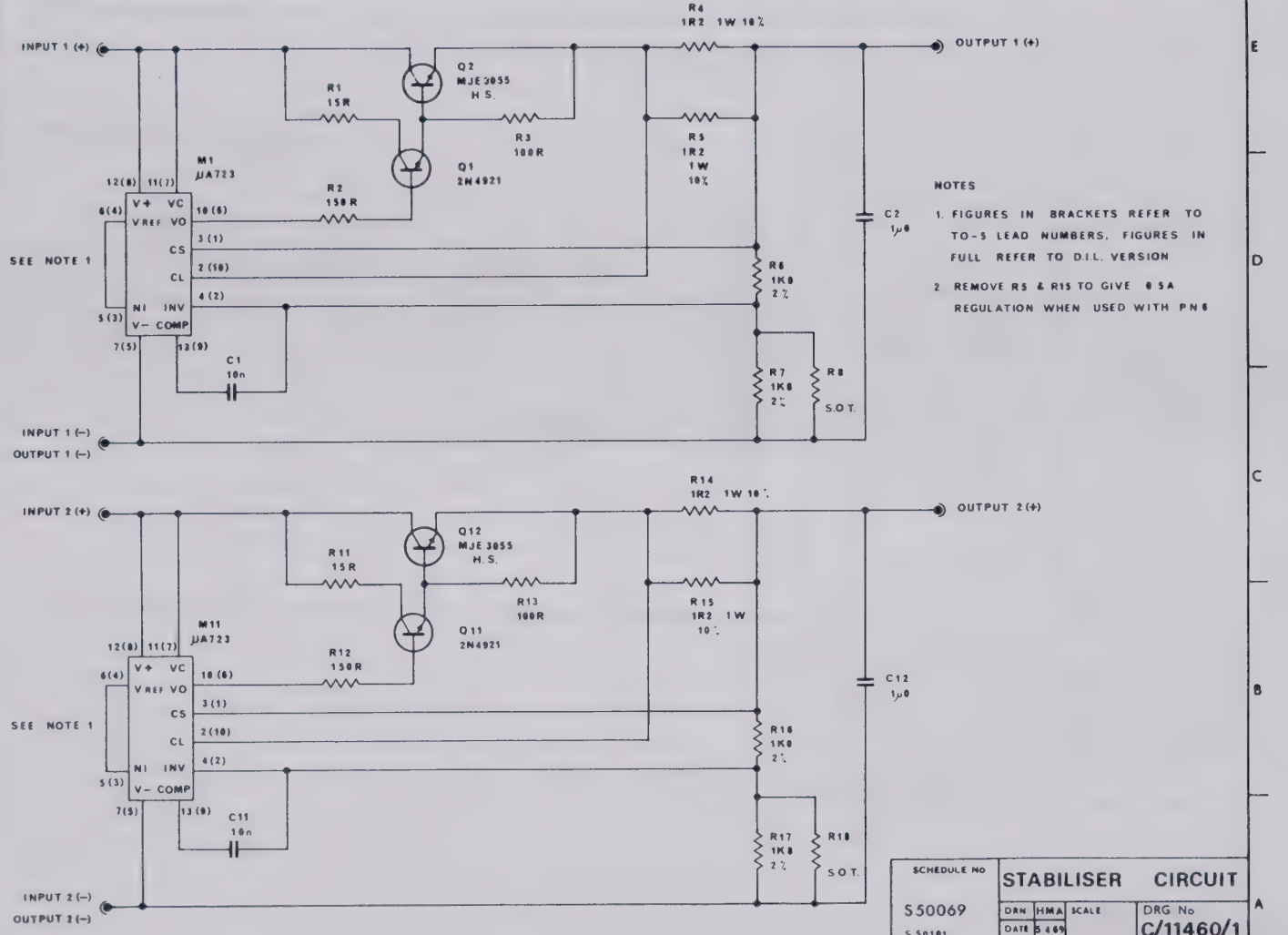
DRG. No.
A4-CD-072-14771-1

SH 1
OF 1


DRG NO
C/11707/1
MODIFICATION
1 30 6 69
2 20 8 69
R4 ADDED
P3/316
3 27 5 70
UP DATED
INCLUDING
MOD NO
P3/375
5 UPDATED To
INCLUDE Mods
3648 440
16-7-75
T1
LP1
12V
VOLTAGE SELECTOR
FS1
SW6
SKT 11
L N E
6.3V
1.2A
MR1
BS6
200 V
100 mA
R5
150K
1W
R1
300R
5W
SEE
NOTE 1
R3
150K
1W
C1
100μ
C2
60μ
22V
4.5A
MR2
6SB10
C3
3m0
50v
R2
10K
FS2
3A ANTI SURGE
17 V
1A
MR3
BS05
C4
2m5
35V
17 V
0.75A
MR4
BS05
C5
2m5
35V
STABILISER
SKT 3
C/11466/1
+240V
+28V
+12V
0V H.C.
0V L.C.
-12V
FOOT SWITCH
POSITIVE GATE
LINE TRIGGER
RV 34
AUDIO GAIN
SKT 6
DISPLAY CRT
HEATERS
CAMERA CRT
HEATERS
SW7
LINE
TRIGGER
TEST
EHT
UNIT
C/11456/1
+28
+12
0V
-2KV
+4KV
R4
10R
SKT4
AUDIO I/P
L.S. 0V
+28V
L.S. O/P
AUDIO
AMP
C/11458/1
LS
15Ω
SKT 10
FOOT
SWITCH
SKT 9
SKT 5
NOTE 1 C1 & C2 IN SAME CAN
SCHEDULE
S58068
S 58101
POWER UNIT
CIRCUIT
DRN
CHK
SCALE
DRG NO
C/11707/1
SPEC
MEDELEC LTD WOKING SURREY

DRG No
C/11460/1

ISSUE	MODIFICATIONS
1	8. 4. 69
6	1 4 71 UP DATED INCLUDING MOD NOS P1/335, P2/385 813 833



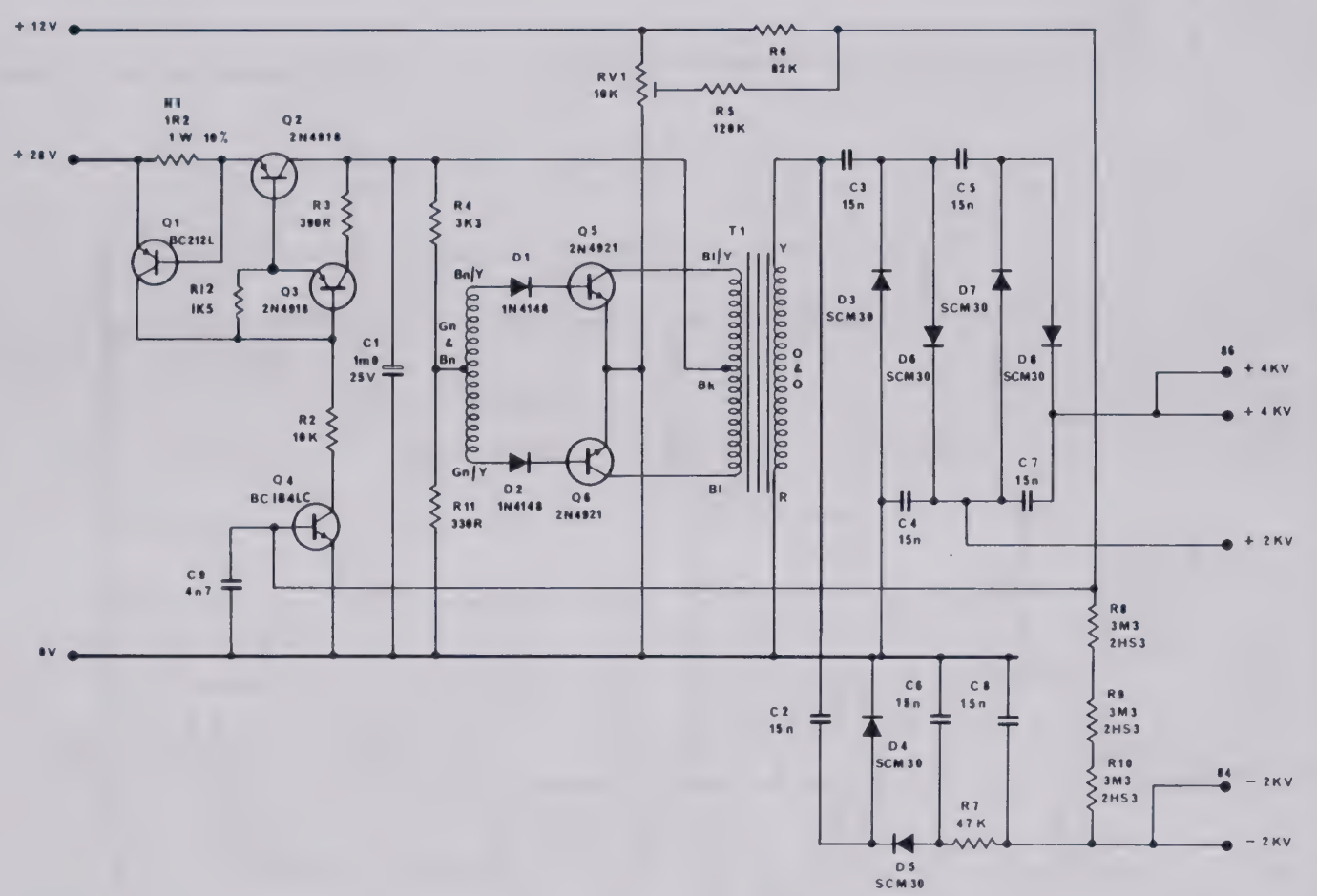
NOTES

1. FIGURES IN BRACKETS REFER TO TO-5 LEAD NUMBERS, FIGURES IN FULL REFER TO D.I.L. VERSION
2. REMOVE R5 & R15 TO GIVE 0.5A REGULATION WHEN USED WITH PN6

SCHEDULE NO	STABILISER CIRCUIT			
S50069	DRN	HMA	SCALE	DRG No C/11460/1
S50101 S50111	DATE	5 4 69		
	CHK.			
SPEC.	MEDELEC LTD. WOKING, SURREY			SIZE 2

DRG No
C/11456/1

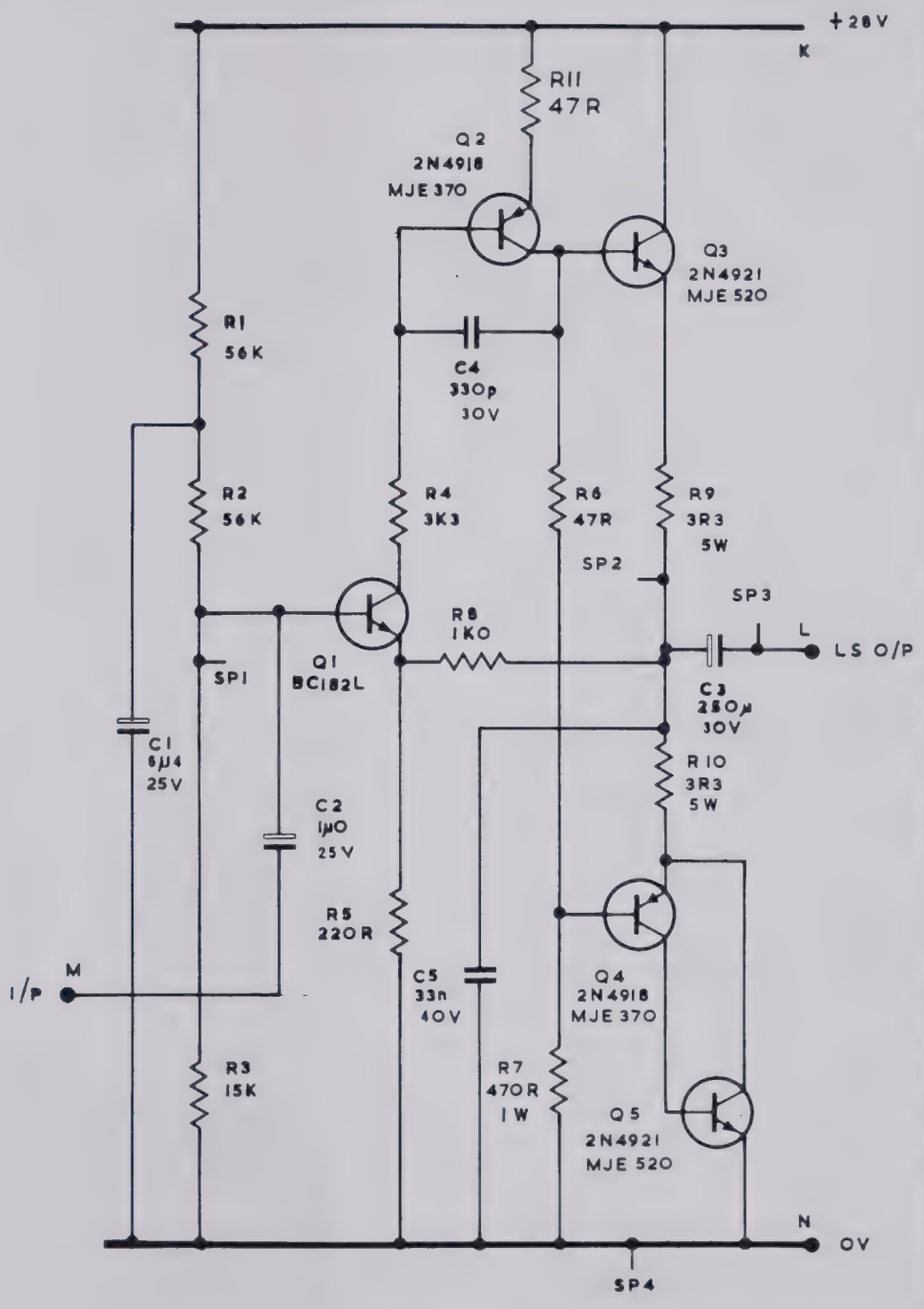
ISSUE	MODIFICATIONS
2	RE DRAWN 3 10 68
7	1 4 71 UP DATED INCLUDING MOD NOS P2/396,P2/365 P1/366,812,824
8	R12 ADDED. Q4 was BC182L. EM64 119



SCHEDULE No.	STABILISED E.H.T. SUPPLY CIRCUIT			
S 50069 S 50101	DRN HMA	SCALE	DRG No C/11456/1	
	DATE 3/10/68			
	CHK			
SPEC.	MEDELEC LTD. WOKING, SURREY			SIZE 2

DRG No.
C/11458/1

ISSUE	MODIFICATIONS
1	17. 9. 69.
2	C1 WAS 10µ C2 " 12V 16TH SEPT 69 P1, 320
3	30 12 69 P2/396
4	RII ADDED EMG6. 456 19-8-75



SCHEDULE No.

S50069
S50101
S50137
S50139

SPEC

AUDIO AMPLIFER MKIII CIRCUIT

DRN.	H.M.A.	SCALE	DRG. No. C/11458/1
DATE	17.9.69		
CHK.			

MEDELEC LTD. WOKING, SURREY.

NH1994

SIZE 1.

ORG No A1-043-14242/1 SH 1 OF 1

IF IN DOUBT - ASK

THIRD ANGLE PROJECTION

DO NOT SCALE

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ATTENUATOR P.C.B. PC-043-14244/2

SKT 1 · C1 150n · SW1 ac / gnd / dc · SW2 a/b · SW2c · SW2d · SW2 e/f

VC4 4-40p · R1 999K · VC1 4-40p · R4 1K0 · C2 8n2

VC5 4-40p · R2 990K 1% · VC2 4-40p · R5 10K1 · C3 820p

VC6 4-40p · R3 900K · VC3 4-40p · R6 111K 1% · C4 82p

VC9 4-40p · R7 806K 1% 0.25W · VC7 4-40p · R9 250K · C5 47p

VC10 4-40p · C20 20p · R8 500K 1% 0.5W · VC8 4-40p · R10 1M0 · C6 20p

TO PIN 1

TO PIN 2

C7 1n0 · R20 8K2 · R16 8K2 · D1 EPAD50 · R25 680R · Q8 · R31 680R · Q14

CA3046 M1 · CA3046 M2

VC11 4-40p · RV3 47K · R38 22K · SW3a · RV4 470K · R39 270K · SW3b

SP1 · SP2

R45 180R · PL1/6 +12V

D8 BZY88C 6V2 · C11 100u · D9

TRIG. OUT PL1/2

PL1/3 O/P

R43 100R · R42 49K9 · C10 330p

R29 10R · RV2 2K0 · R30 1K2 · C9 5n0 · R32 6K8 · R34 6K8 · R22 6K8 · R24 6K8 · R26 9K1 1%

R36 6K8 · R35 2K7 · R33 330R · R28 3K9 · R37 562K · R40 3M3 · R41 3K9 · RV5 220K · RV6 1M0 · C12 100u

D10 · D11 BZY88C 6V2

R46 180R · PL1/5 -12V

C13 20p · R12 100K 2W · R13 9K1 1% · R14 100R · Q1a · Q1b · E410 · RV1 200R CERMET · R11 1M0 1% · D2 EPAD50

R18 4K7 · D3 · R19 1K0 1% · R21 47K · RV7 100K CERMET · C14 1n0 · R15 6K19 · R17 6K19

PART OF M1 · R23 330R · R47 499R 1% · D4

PART OF M2 · D6

0V

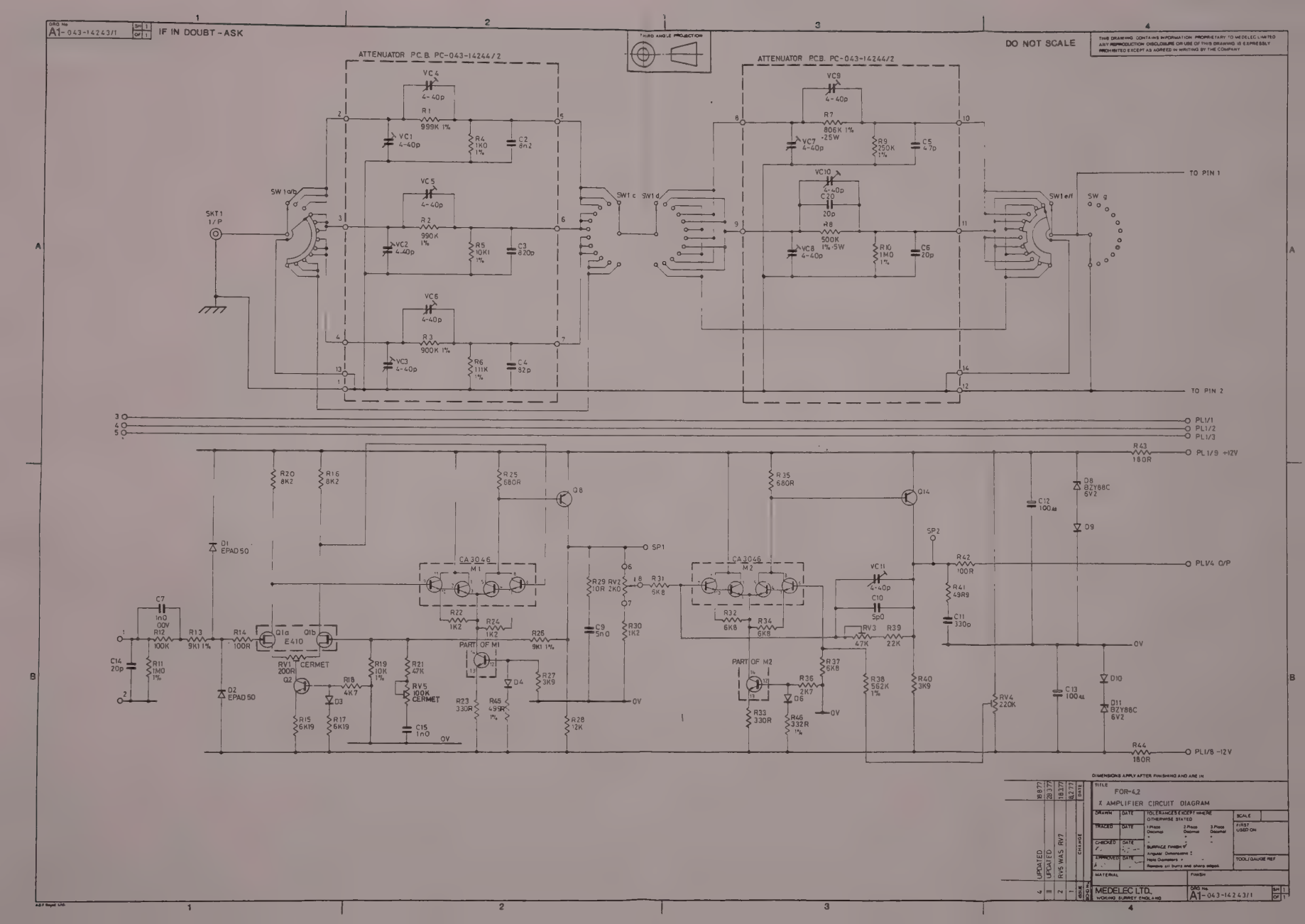
DIMENSIONS APPLY AFTER FINISHING AND ARE IN

TITLE	FOR-4.2 Y AMPLIFIER CIRCUIT DIAGRAM				
DRAWN C.C-B	DATE 12-8-76	TOLERANCES EXCEPT WHERE OTHERWISE STATED			SCALE
TRACED	DATE	1 Place Decimal ±	2 Place Decimal ±	3 Place Decimal ±	FIRST USED ON
CHECKED	DATE	SURFACE FINISH			
APPROVED	DATE	Angular Dimensions ± Hole Diameters + Remove all burrs and sharp edges			TOOL/GAUGE REF
MATERIAL		FINISH			

CHANGE: 2 28.3.77 · 1 8.2.77 · DATE · SPEC No

MEDELEC LTD. WOKING SURREY ENGLAND

ORG No A1-043-14242/1 QT 1 1


ORG No A1-043-14243/1
SH 1 OF 1
IF IN DOUBT - ASK
THIRD ANGLE PROJECTION
DO NOT SCALE
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ATTENUATOR P.C.B. PC-043-14244/2
ATTENUATOR P.C.B. PC-043-14244/2
SKT1 I/P
SW 1a/b
SW 1c
SW 1d
SW 1e/f
SW g
TO PIN 1
TO PIN 2
VC4 4-40p
R1 999K 1%
VC1 4-40p
R4 1K0 1%
C2 8n2
VC5 4-40p
R2 990K 1%
VC2 4-40p
R5 10K1 1%
C3 820p
VC6 4-40p
R3 900K 1%
VC3 4-40p
R6 111K 1%
C4 82p
VC9 4-40p
R7 806K 1% .25W
VC7 4-40p
R9 250K 1%
C5 47p
VC10 4-40p
C20 20p
R8 500K 1% .5W
VC8 4-40p
R10 1M0 1%
C6 20p
PL1/1
PL1/2
PL1/3
PL1/9 +12V
PL1/4 O/P
PL1/8 -12V
R43 180R
R42 100R
R41 49R9
C11 330p
C12 100µ
D8 BZY88C 6V2
D9
D10
D11 BZY88C 6V2
C13 100µ
SP1
SP2
0V
CA3046 M1
CA3046 M2
PART OF M1
PART OF M2
Q8
Q14
Q1a Q1b E410
Q2
D1 EPAD50
D2 EPAD50
D3
D4
D6
R20 8K2
R16 8K2
R25 680R
R35 680R
R29 RV2 10R 2K0
R31 5K6
R30 1K2
R22 1K2
R24 1K2
R32 6K8
R34 6K8
R26 9K1 1%
R27 3K9
R28 12K
R37 6K8
R36 2K7
R38 562K 1%
R40 3K9
R39 22K
RV3 47K
VC11 4-40p
C10 5p0
C9 5n0
R12 100K
R13 9K1 1%
R14 100R
R11 1M0 1%
C14 20p
C7 1n0 100V
RV1 200R CERMET
R18 4K7
R19 10K 1%
R21 47K
RV5 100K CERMET
R15 6K19
R17 6K19
C15 1n0
R23 330R
R45 499R 1%
R33 330R
R46 332R 1%
RV4 220K
DIMENSIONS APPLY AFTER FINISHING AND ARE IN
TITLE
FOR-42
X AMPLIFIER CIRCUIT DIAGRAM
DRAWN DATE
TRACED DATE
CHECKED DATE
APPROVED DATE
TOLERANCES EXCEPT WHERE OTHERWISE STATED
1 Place Decimal ± 2 Place Decimal ± 3 Place Decimal ±
SURFACE FINISH
Angular Dimensions ±
Hole Diameters +
Remove all burrs and sharp edges.
SCALE
FIRST USED ON
TOOL/GAUGE REF
MATERIAL
FINISH
4 UPDATED 18.8.77
3 UPDATED 28.3.77
2 RV5 WAS RV7 18.3.77
1 ISSUE 8.2.77
DATE
CHANGE
ISS
MEDELEC LTD.
WOKING SURREY ENGLAND
ORG No A1-043-14243/1
SH 1 OF 1

DRG No A1-CD-043-14245/1 | SH | OF

IF IN DOUBT - ASK

DO NOT SCALE

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ALL TRANSISTORS BC182L OR BC212L.
ALL DIODES 1N4148.
ALL RESISTORS 1/4W 5%.
UNLESS OTHERWISE STATED

PL1/15 TB CONTROL
PL1/16 + GATE
PL1/3/9 +12V
PL1/28 XY GATE
PL1/9 0V
PL1/18 FOOT SWITCH
PL1/10 -12V
PL1/3&4 +28V
PL1/15 TIME BASE
PL1/27 Z MOD OUT

EXT TRIG SKT 1
Z MOD IN SKT 3
EXT GATE (REAR PANEL) SKT 4
SW7a/b PART OF SW1 X AMP MODULE @ TERMS: 3R X AMP PCB

PCB 043 14756

INT TRIG. GAIN CONTROL PCB

Y1 TRIG PL2/12
Y2 TRIG PL2/13
Y3 TRIG PL2/14
Y4 TRIG PL2/15

EXT TRIGGER BUFFER AMPLIFIER
TRIGGER BUFFER AMPLIFIER
+VE/-VE PEAK DETECTOR
LEVEL SHIFT CONTROLS
TIME BASE CONTROL

TRIGGER DIFFERENTIAL AMP
LEVEL SHIFT BUFFER AMP
SCHMITT TRIG BUFFER AMP
SCHMITT TRIGGER
TRIGGER GATING
INPUT VERIFICATION MONOSTABLE

AMP CAL SKT 2

PL2/9
PL2/8
PL2/7
PL2/6
PL2/4
PL2/3
PL2/2
PL2/1
0V

PL1/23 Y1 SIG O/P
PL1/24 Y2 SIG O/P
PL1/25 Y3 SIG O/P
PL1/26 Y4 SIG O/P
PL1/11 AMP CAL
PL1/29 X SIG O/P
PL1/31 -12V
PL1/32 0V
PL1/33/34 +12V

DIMENSIONS APPLY AFTER FINISHING AND ARE IN

DRAWN	DATE	TOLERANCES EXCEPT WHERE OTHERWISE STATED			SCALE
TRACED	DATE	1 Place Decimal	2 Place Decimal	3 Place Decimal	FIRST USED ON
CHECKED	DATE	SURFACE Finish of Angular Dimensions ±			TOOL/GAUGE REF
APPROVED	DATE	Hole Diameters + Remove all burrs and sharp edges.			
MATERIAL		FINISH			

MEDELEC LTD. WOKING SURREY ENGLAND

DRG No A1-CD-043-14245/1 | SH | OF

TITLE: FOR 4-2 TRIGGER CIRCUIT DIAGRAM

DMS 5-662 | ISSUE | CHANGE | DATE

DRG No A1-043-14851 SH OF

IF IN DOUBT - ASK

THIRD ANGLE PROJECTION

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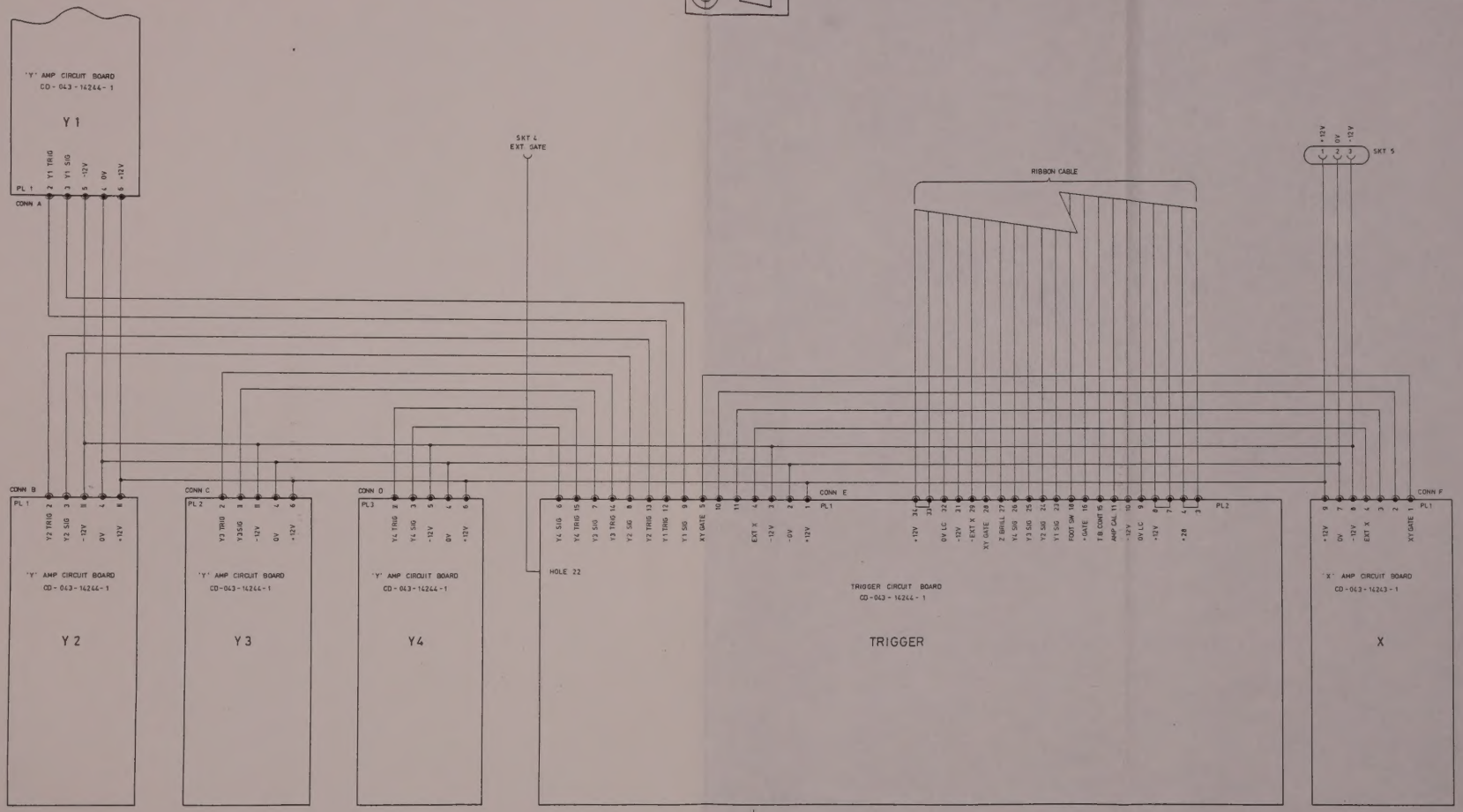

DIMENSIONS APPLY AFTER FINISHING AND ARE IN

TITLE

FOR 4.2
GENERAL CIRCUIT DIAGRAM

DRAWN W S	DATE 18-8-77	TOLERANCES EXCEPT WHERE OTHERWISE STATED	SCALE
TRACED	DATE	1 Place Decimal ± / 2 Place Decimal ± / 3 Place Decimal ±	FIRST USED ON
CHECKED	DATE 19/8/77	SURFACE FINISH / Angular Dimensions ± / Hole Diameters + - Remove all burrs and sharp edges.	
APPROVED	DATE		TOOL/GAUGE REF
MATERIAL		FINISH	

ISSUE	DATE	CHANGE	BY
1	8.9.77		

MEDELEC LTD.
WOKING, SURREY, ENGLAND

DRG No A1-043-14851 SH 1 OF 1

MP MASTER
MA23324